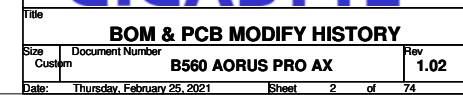
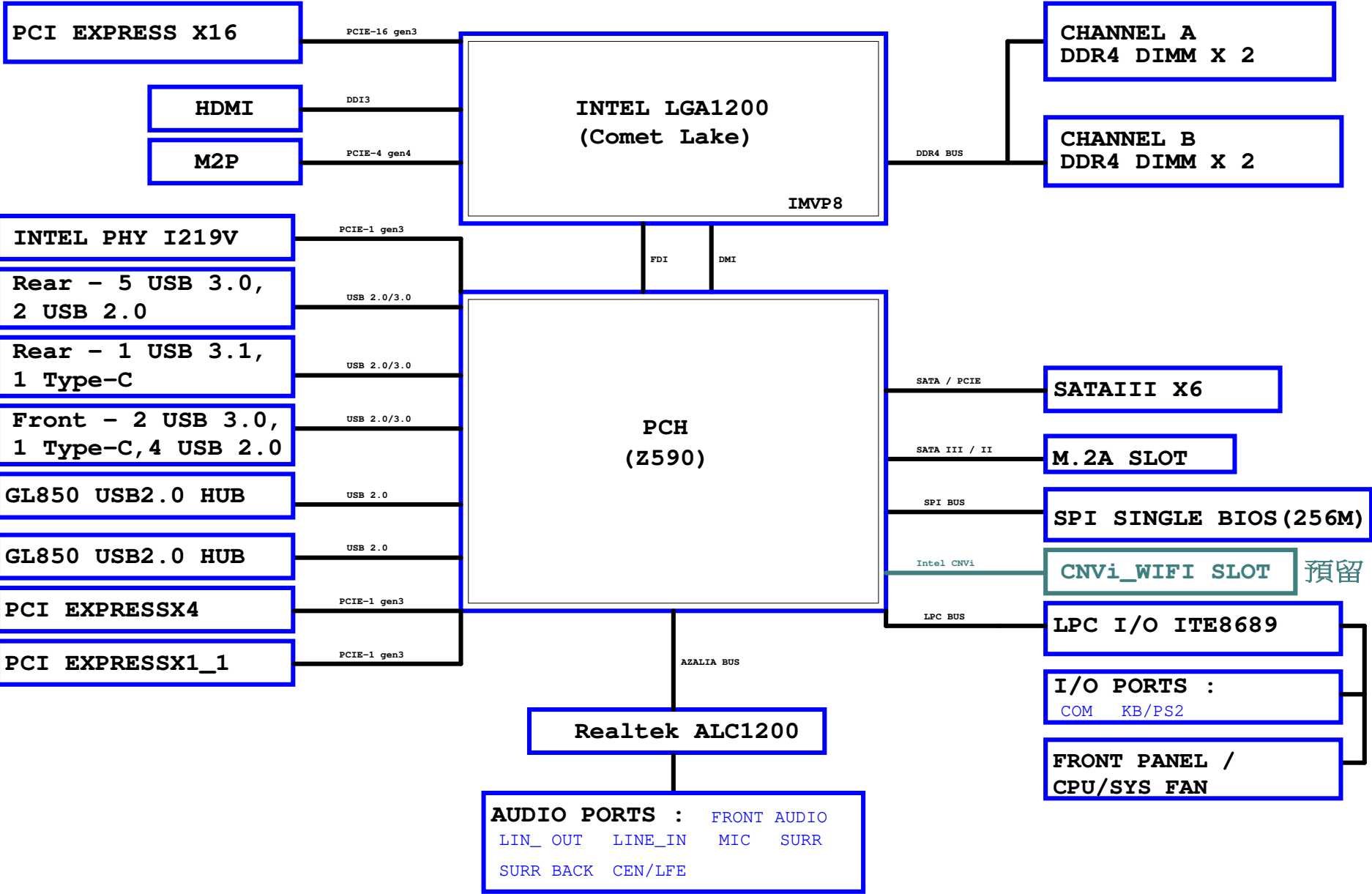


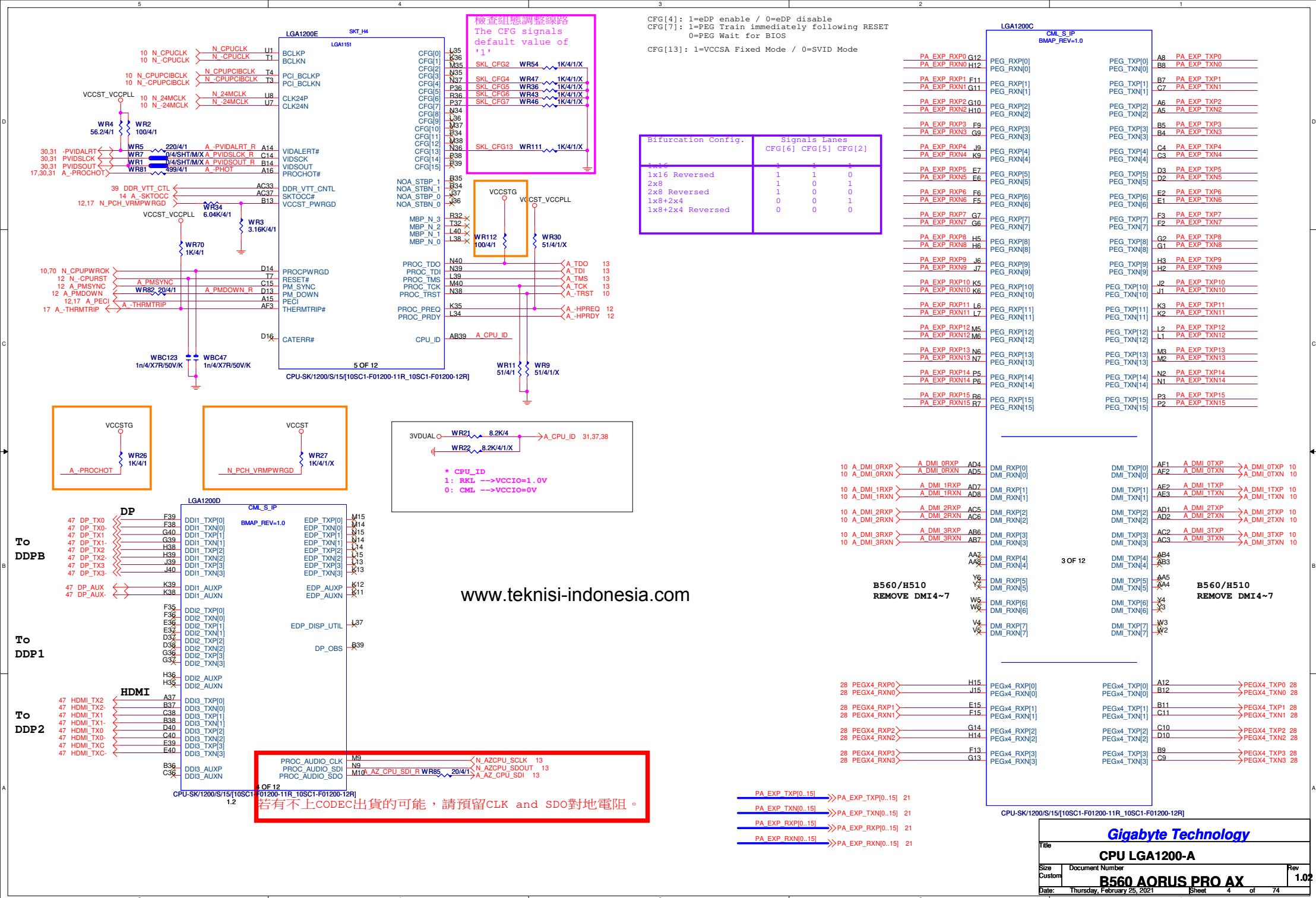
Circuit or PCB layout change

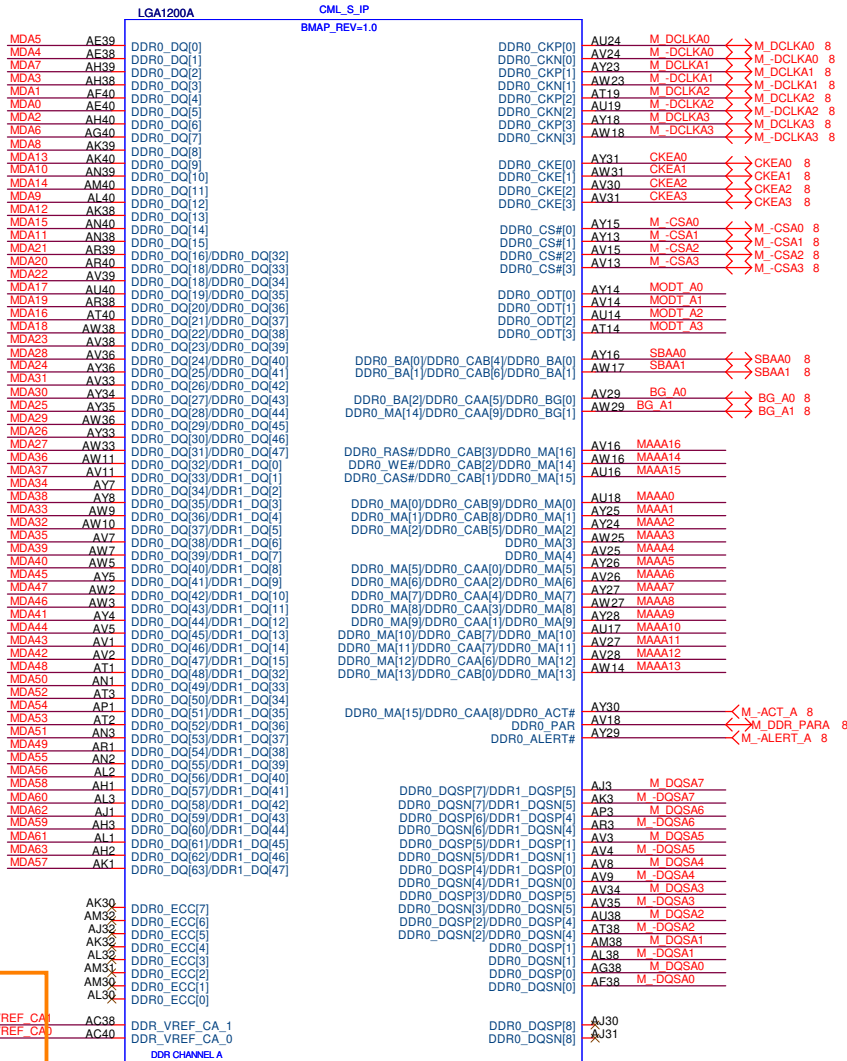
2020/09/02

[illegible]

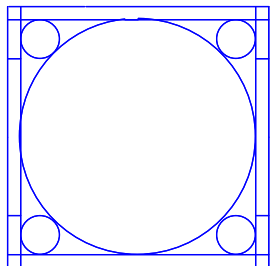
BLOCK DIAGRAM







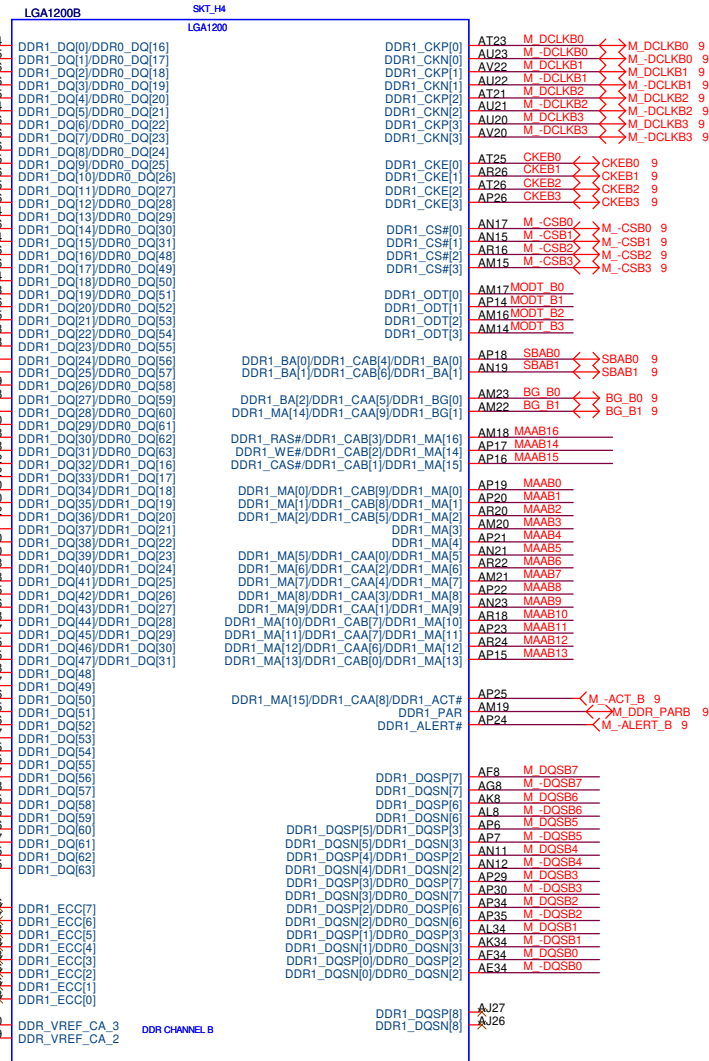
CPU-SK/1200/S/15[10SC1-F01200-11R_10SC1-F01200-12R]



黑色cover

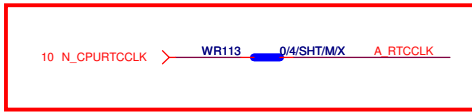
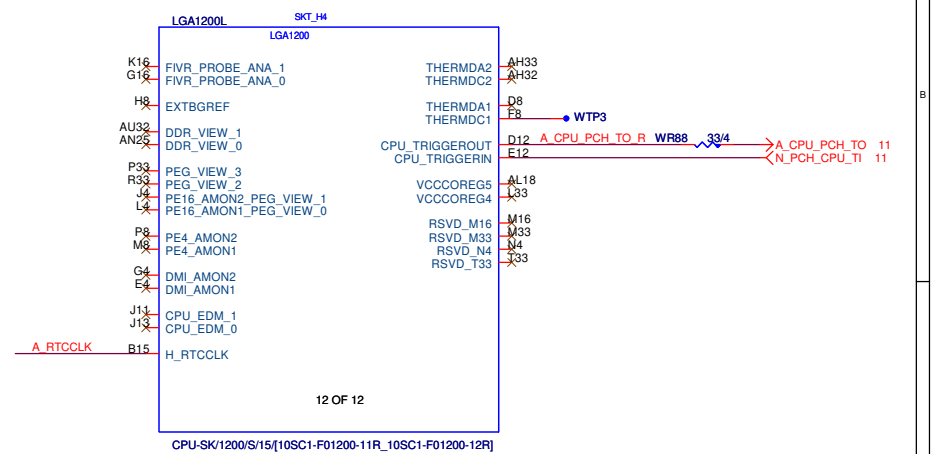
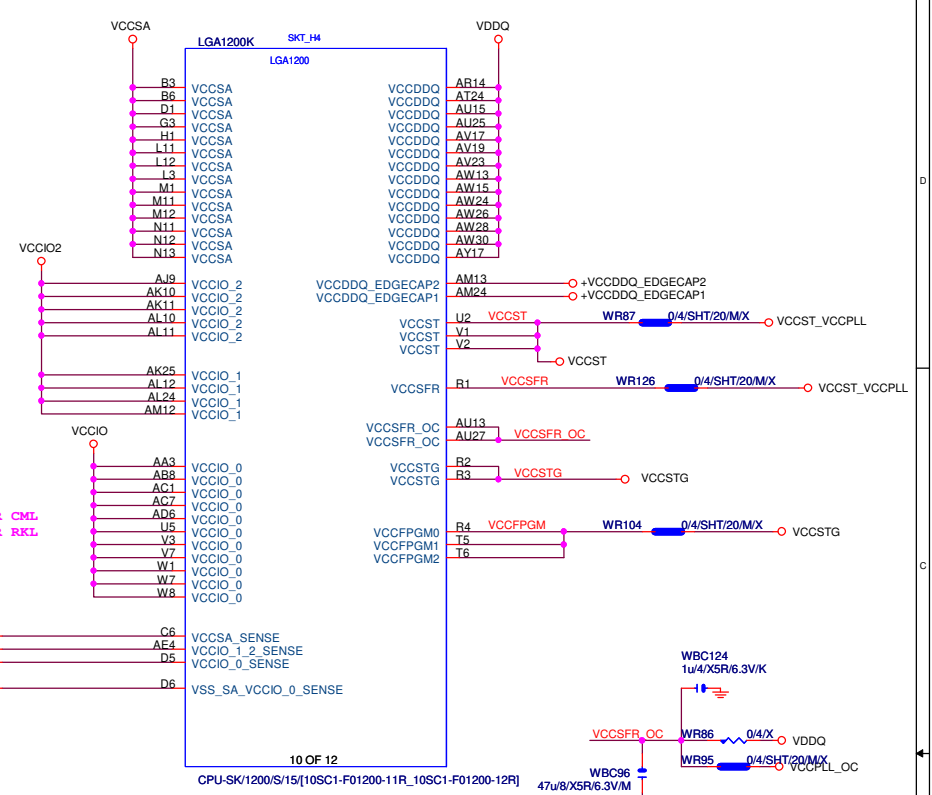
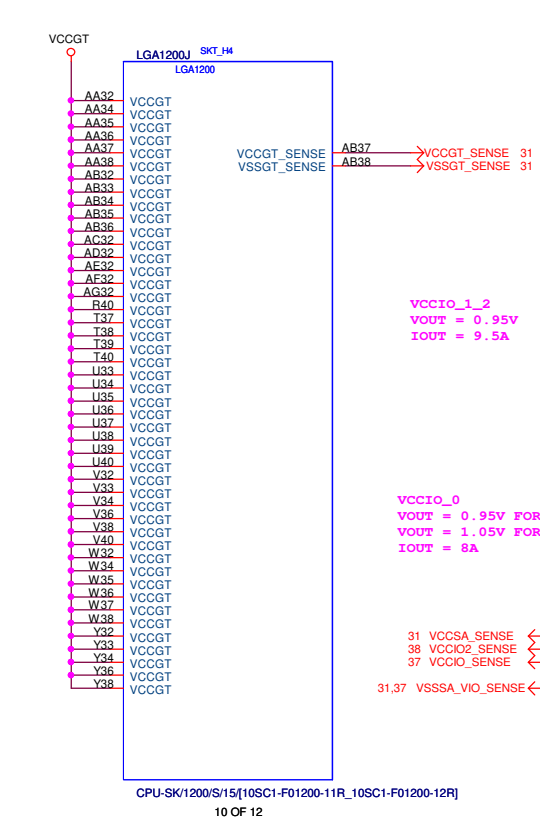
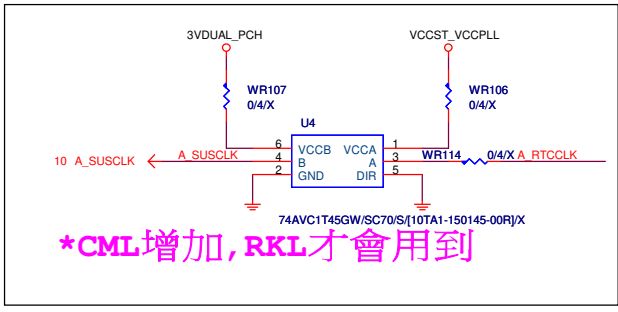
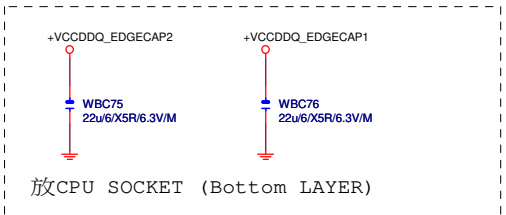
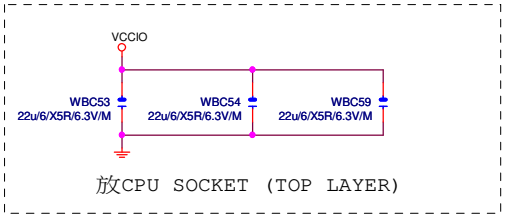
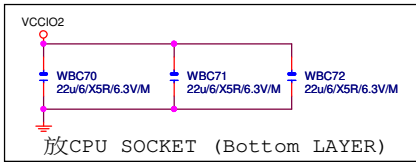
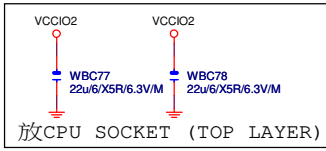
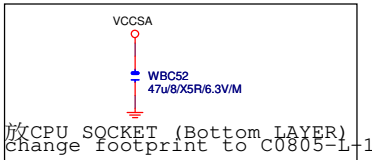
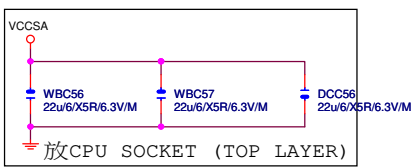
LGA1200
ILM_BP_CR/1200/BKN[12KRC-SF0001-C1R_12KRC-SF0001-C2R]

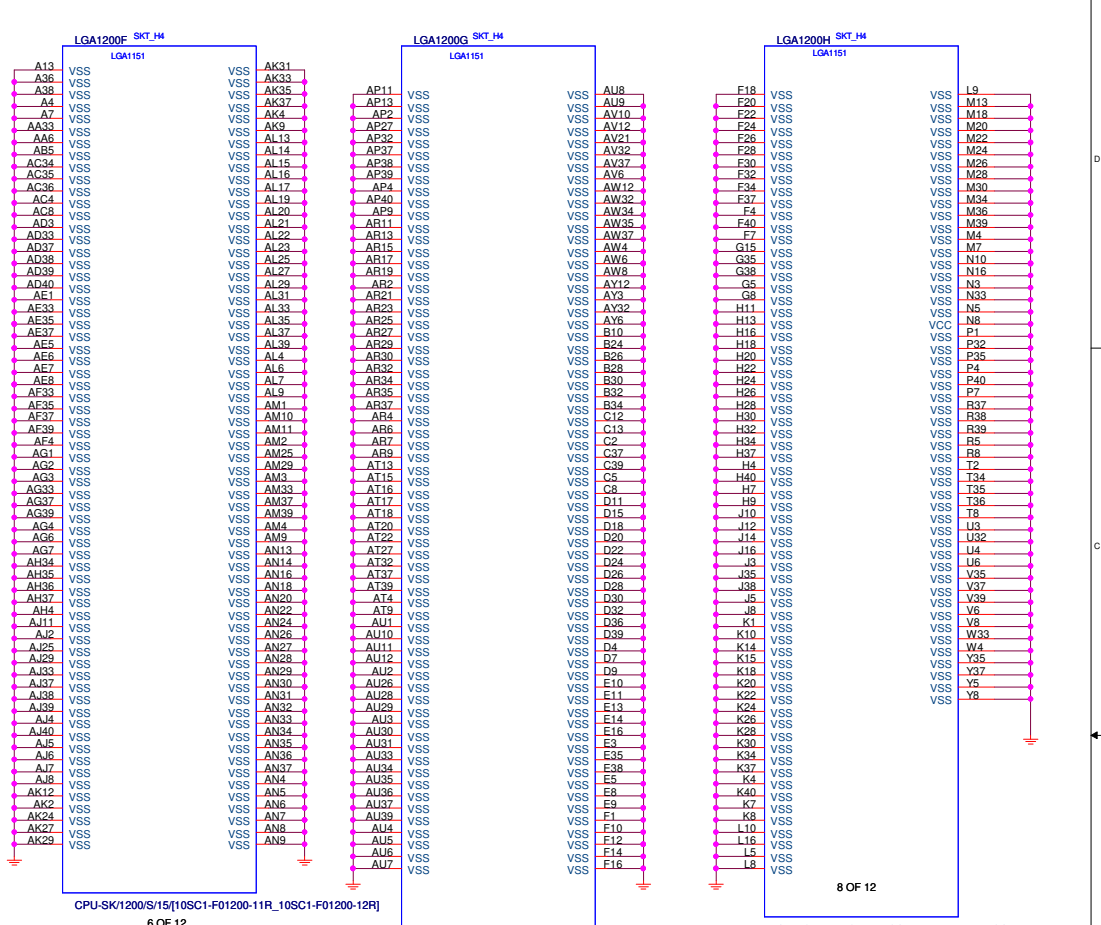
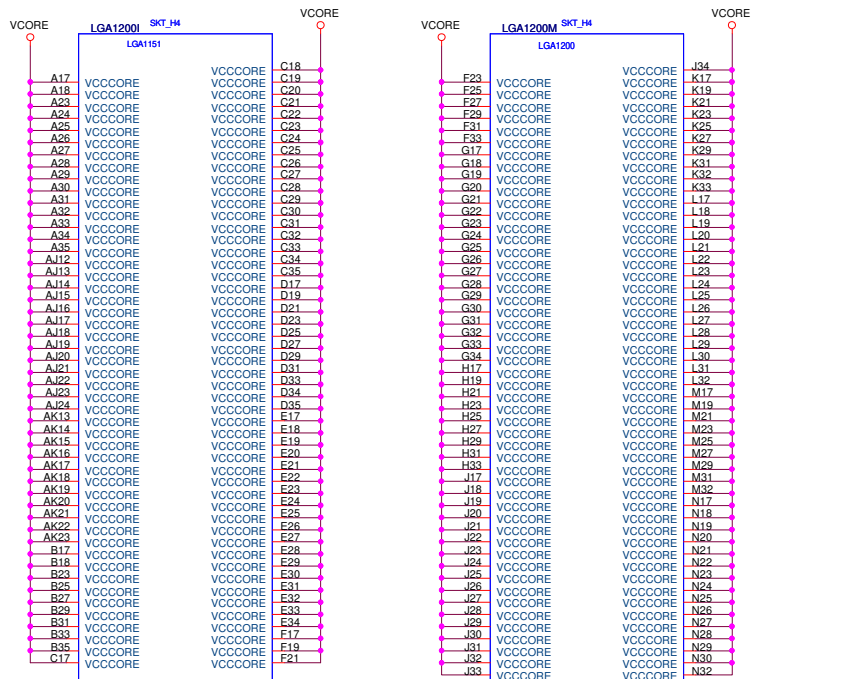
9 VREF_CA3
9 VREF_CA2



CPU-SK/1200/S/15[10SC1-F01200-11R_10SC1-F01200-12R]

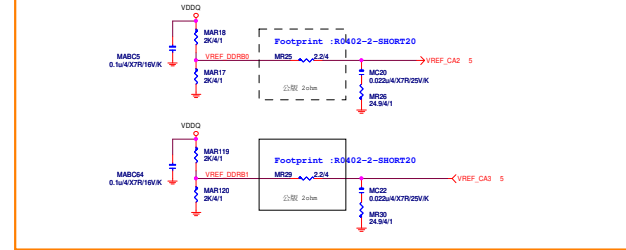
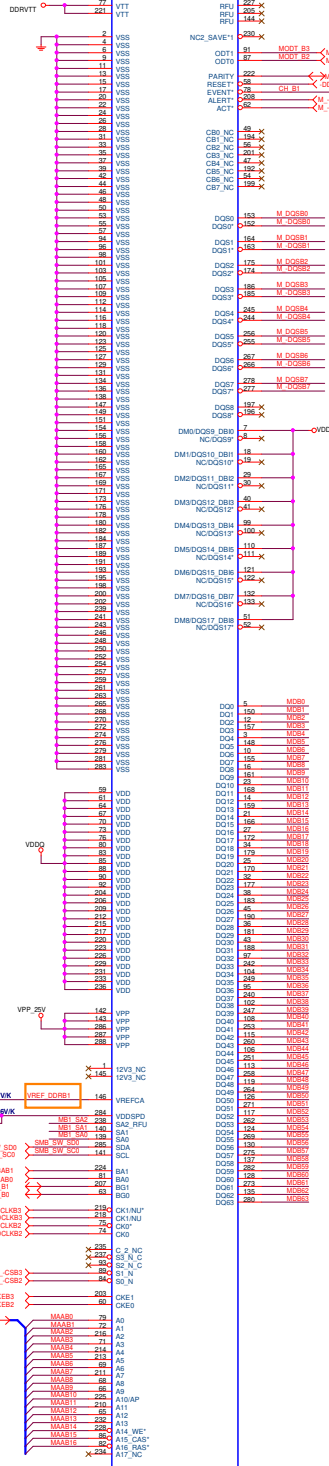
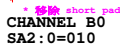
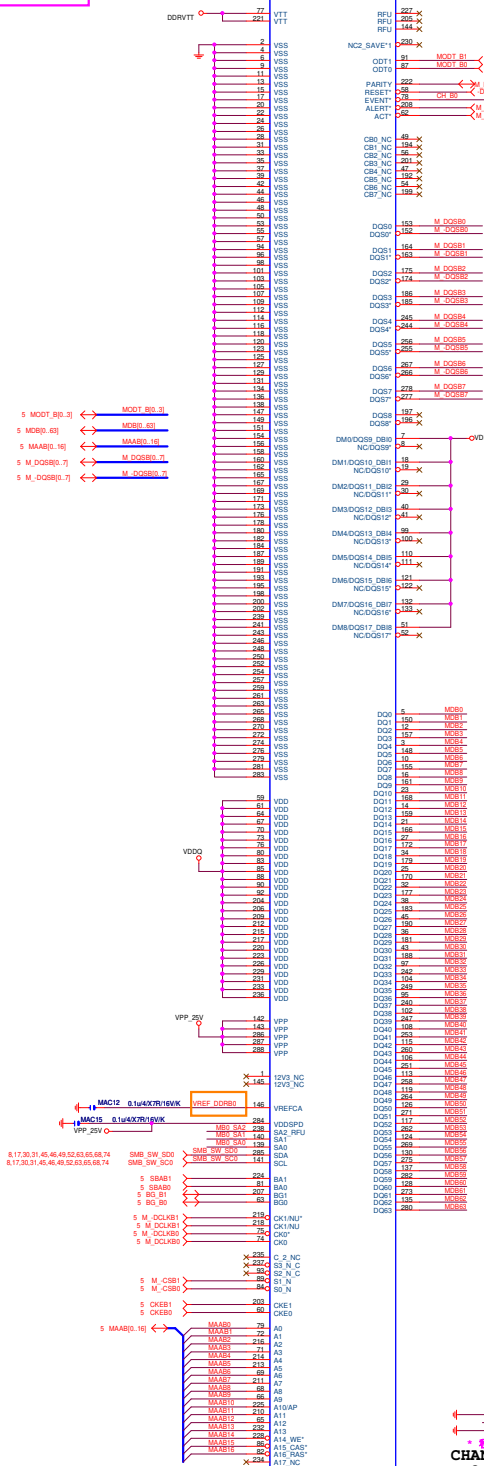
8 MODT_A[0..3] ↔ MODT_A[0..3]
9 MODT_B[0..3] ↔ MODT_B[0..3]
8 MDA[0..63] ↔ MDA[0..63]
9 MDB[0..63] ↔ MDB[0..63]
8 M_DQSA[0..7] ↔ M_DQSA[0..7]
8 M_DQSA[0..7] ↔ M_DQSA[0..7]
8 MAA[0..16] ↔ MAA[0..16]
9 MAAB[0..16] ↔ MAAB[0..16]
9 M_DQSB[0..7] ↔ M_DQSB[0..7]
9 M_DQSB[0..7] ↔ M_DQSB[0..7]





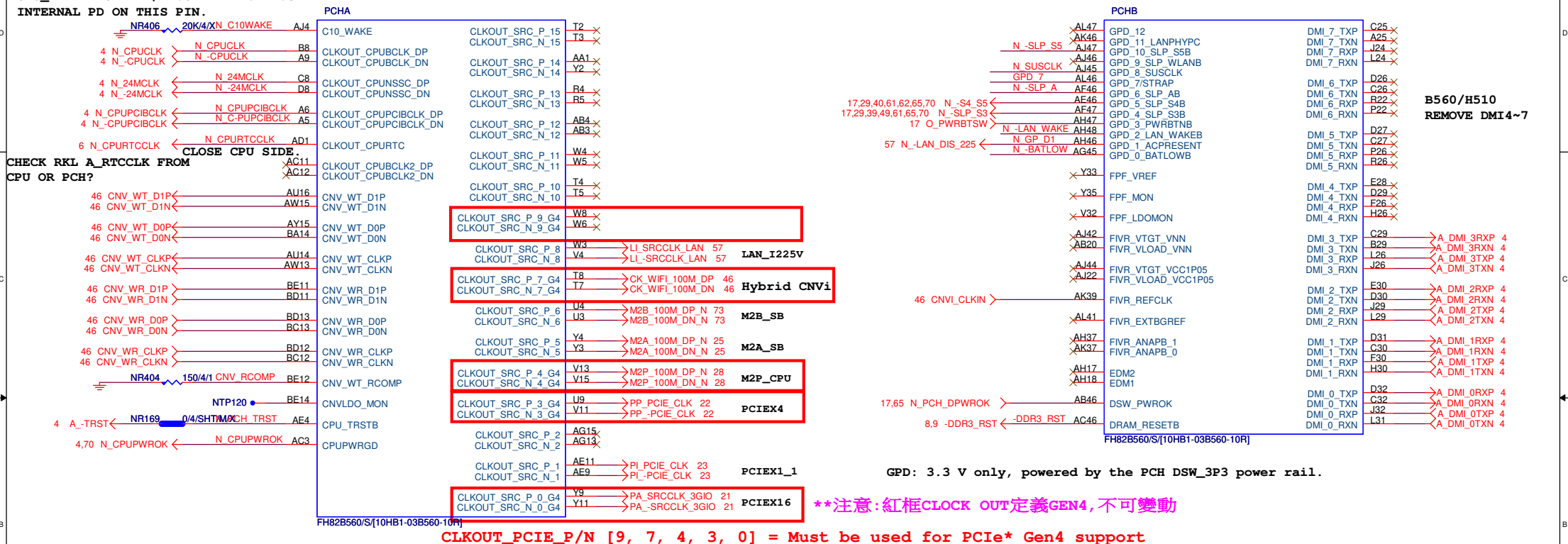
* 刪 Vcore 電容

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RKL_TGP_PCH-H R0.1

C10_WAKE RESERVED/BIOS NEED TO PROGRAM
INTERNAL PD ON THIS PIN.

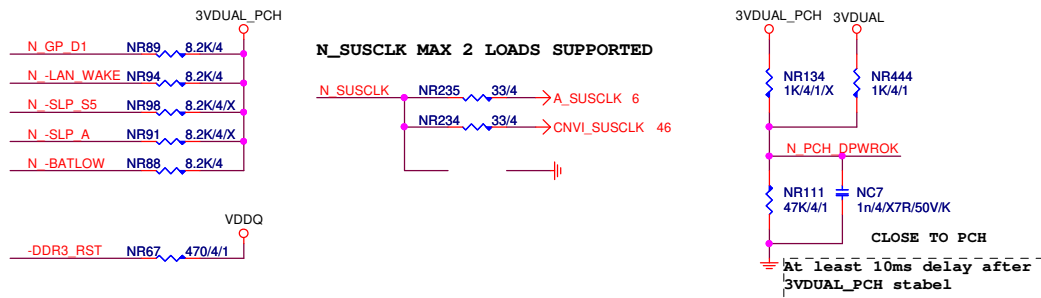


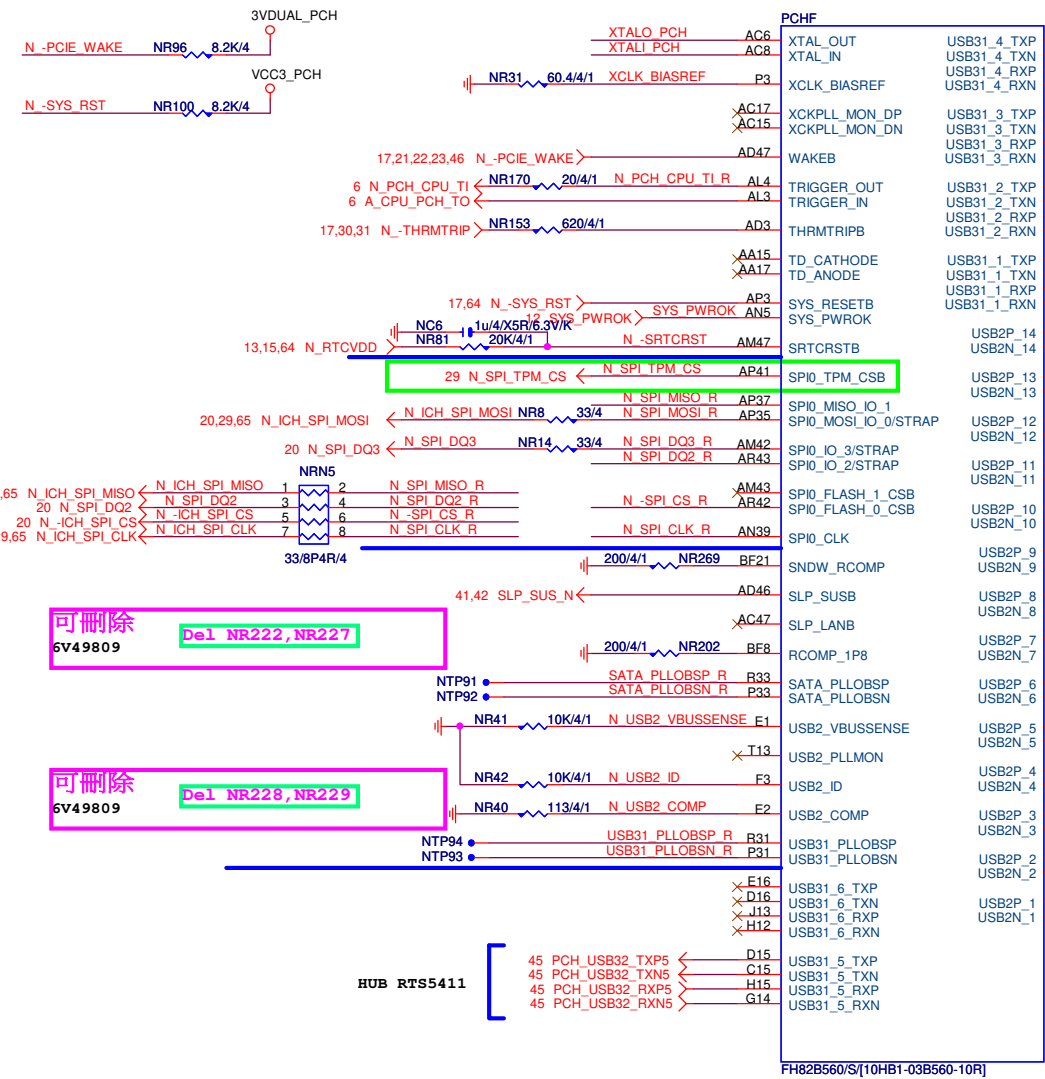
STRAP

3VDUAL_PCH

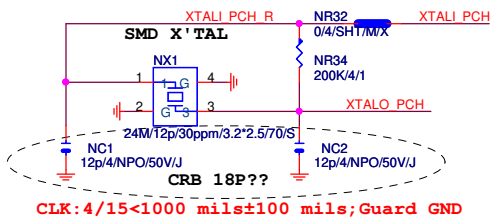
GPD 7 NR237 100K4/X

Reserved.This strap should sample LOW.INTERNAL PD.



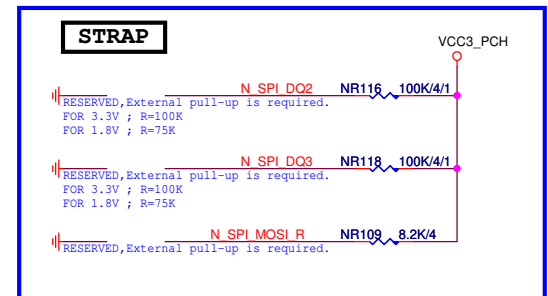


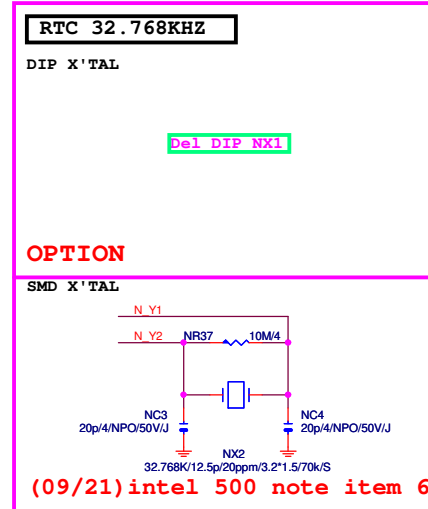
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Intel 500 series PCH USB configuration P1~P6						
ITEM	USB P1	USB P2	USB P3	USB P4	USB P5	USB P6
H510	U3.2 Gen1x1	U3.2 Gen1x1	U3.2 Gen1x1	U3.2 Gen1x1	NA	NA
B560	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
H570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	Gen2x2		Gen2x2		Gen2x2	

Intel 500 series PCH USB20 configuration						
ITEM	USB P1~9	USB P10	USB P11	USB P12	USB P13	USB P14
H510	USB2	NA	NA	NA	NA	For Intel® Wireless- AC
B560	USB2	USB2	USB2	NA	NA	
H570	USB2	USB2	USB2	USB2	USB2	
Z590	USB2	USB2	USB2	USB2	USB2	
Q570	USB2	USB2	USB2	USB2	USB2	
W580	USB2	USB2	USB2	USB2	USB2	

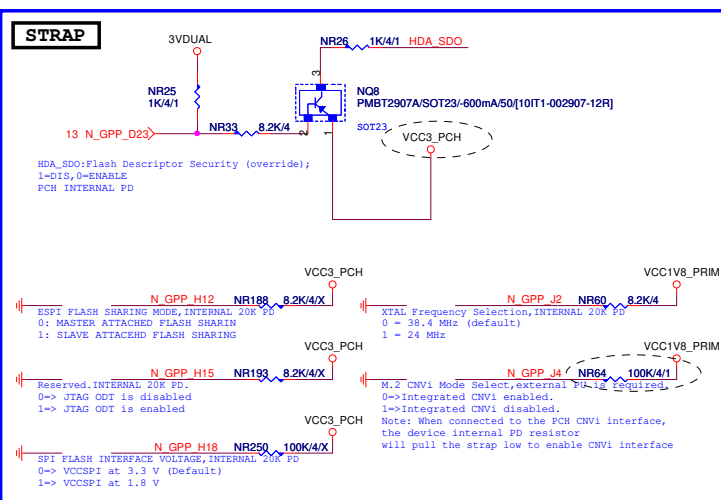
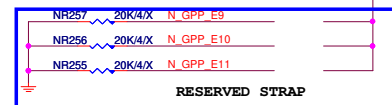
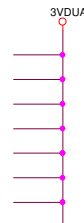
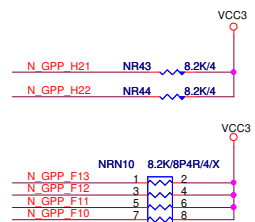
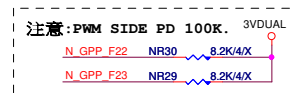
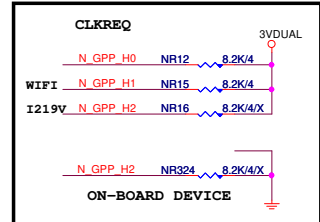




Intel 500 series PCH PCIE P13~P24												
ITEM	PCIE P13	PCIE P14	PCIE P15	PCIE P16	PCIE P17	PCIE P18	PCIE P19	PCIE P20	PCIE P21	PCIE P22	PCIE P23	PCIE P24
H510	SATA_0 /Gbe	SATA_1	SATA_2	SATA_3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B560	SATA_0 /Gbe	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	N/A	N/A	PCIE	PCIE	PCIE	PCIE
H570	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Z590	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Q570	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
W580	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE SATA_6	PCIE SATA_7	PCIE	PCIE	PCIE	PCIE
					Intel® RST for x2/x4 M.2				Intel® RST for x2/x4 M.2			

Intel 500 series PCH USB P7-P10				
ITEM	USB P7	USB P8	USB P9	USB P10
H510	NA	NA	NA	NA
B560	NA	NA	NA	NA
H570	U3.2 Gen1x1	U3.2 Gen1x1	PCIE	PCIE
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
	PCIE	PCIE	PCIE	PCIE
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE

RKL_TGP_PCH-H R0.1



Fixed voltage on certain GPIO groups: GPD (3.3 V), GPP_J and GPP_S (1.8 V/VCCPRIM_1P8)

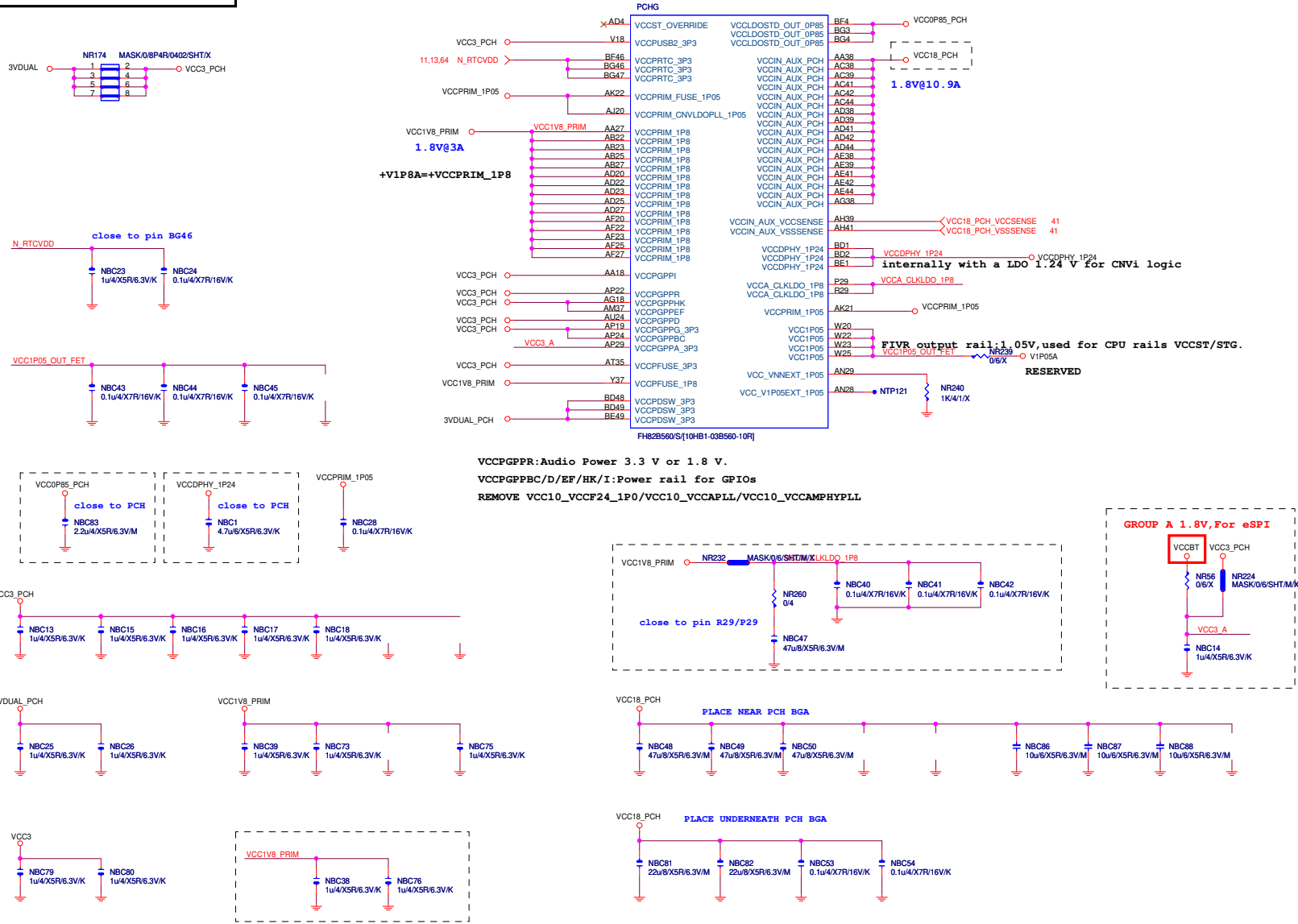
Display Port DDC/HOT PLUG SIGNAL		
CPU PORT	PCH DDC	PCH HPD
DDI_A/EDP	GPP_G0/G1	GPP_K6
DDI_1/B	GPP_I5/I6	GPP_K7
DDI_2/C	GPP_G12/G13	GPP_I1
DDI_3/D	GPP_G14/G15	GPP_I2

PCH Signal Glitch Free



HPD: DDI*. PULL HI IF NO USE.

A N_GPP_K6 NR233 100K/4/1
B N_GPP_K7 NR236 100K/4/1/X DP
 N_GPP_K10 NR273 100K/4/1
C N_GPP_I1 NR238 100K/4/1
D N_GPP_I2 NR270 100K/4/1/X HDMI
 N_GPP_I3 NR272 100K/4/1
 N_GPP_I4 NR271 100K/4/1

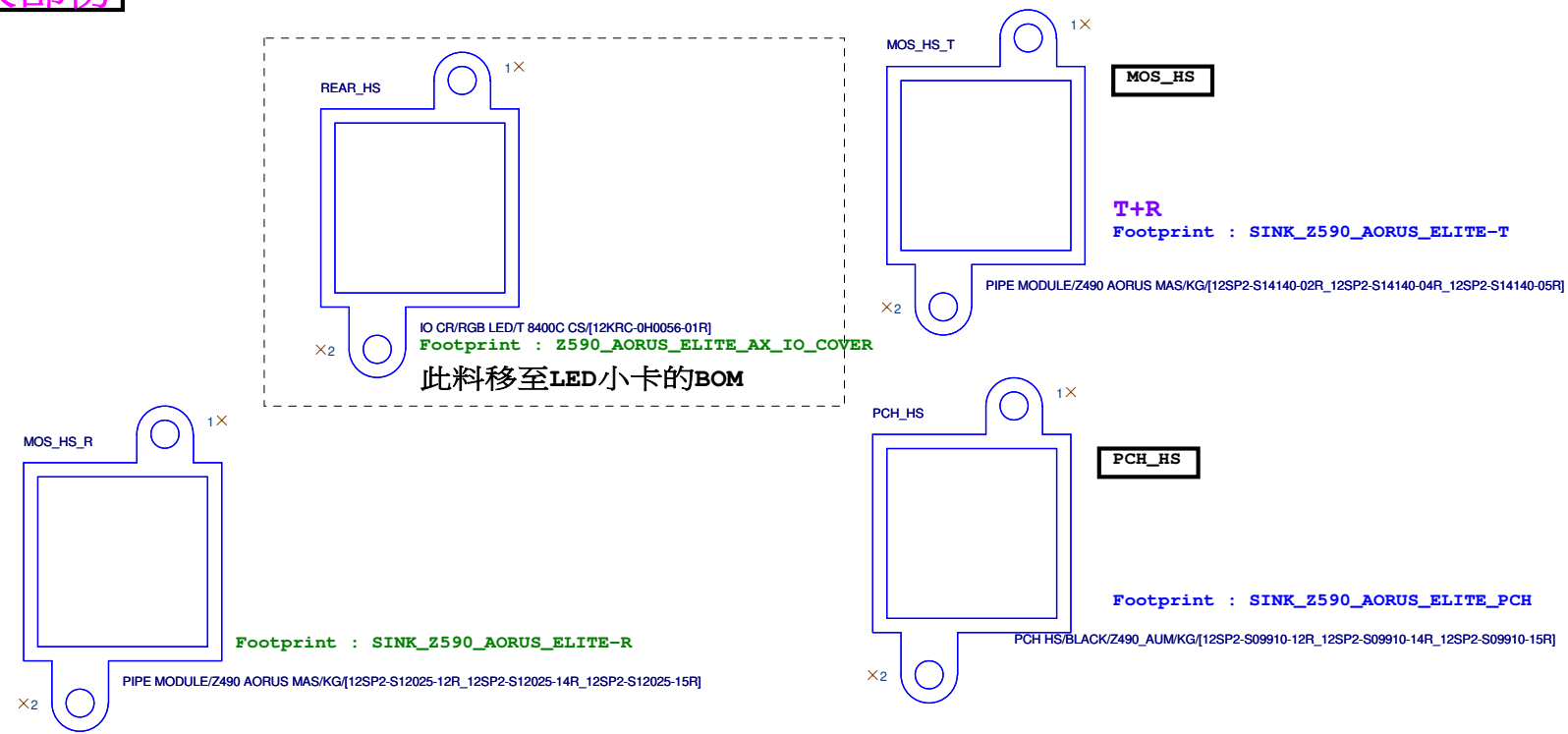


PCHH			PCHI			
AW2S	VSS	VSS	F42	A17	VSS	A123
AW3S	VSS	VSS	F8	A2	VSS	A125
AY2S	VSS	VSS	F1	A28	VSS	A127
AY3S	VSS	VSS	G41	A3	VSS	A128
AY4S	VSS	VSS	G48	A33	VSS	A129
AY7	VSS	VSS	G49	A37	VSS	AK17
B1	VSS	VSS	G9	A4	VSS	AK18
B2	VSS	VSS	G25	A41	VSS	AK19
B4	VSS	VSS	H43	A45	VSS	AK25
B46	VSS	VSS	H8	A46	VSS	AK26
B48	VSS	VSS	J11	A47	VSS	AK28
B49	VSS	VSS	J25	A49	VSS	AK29
B6	VSS	VSS	J39	AA12	VSS	AK30
BA41	VSS	VSS	J9	AA13	VSS	AK32
BA43	VSS	VSS	J11	AA20	VSS	AK33
BA9	VSS	VSS	K39	AA22	VSS	AK35
BB26	VSS	VSS	K45	AA23	VSS	AK38
BB44	VSS	VSS	K5	AA25	VSS	AK45
BB8	VSS	VSS	L14	AA29	VSS	AK50
BC11	VSS	VSS	L25	AA30	VSS	AL19
BC15	VSS	VSS	M12	AA32	VSS	AL22
BC19	VSS	VSS	M17	AA33	VSS	AL23
BC24	VSS	VSS	M19	AA35	VSS	AL25
BC26	VSS	VSS	M21	AA37	VSS	AL26
BC28	VSS	VSS	M22	AA49	VSS	AL28
BC31	VSS	VSS	M24	A45	VSS	AL29
BC33	VSS	VSS	M25	AB28	VSS	AL31
BC35	VSS	VSS	M26	AC13	VSS	AM1
BC39	VSS	VSS	M28	AC18	VSS	AM12
BC41	VSS	VSS	M29	AC35	VSS	AM17
BC9	VSS	VSS	M31	AC37	VSS	AM33
BF13	VSS	VSS	M33	AC4	VSS	AM35
BF2	VSS	VSS	M39	AC45	VSS	AM38
BF42	VSS	VSS	M6	AC5	VSS	AM49
BF48	VSS	VSS	M6	AC9	VSS	AN17
BF49	VSS	VSS	P11	AD11	VSS	AN19
BF67	VSS	VSS	P21	AD12	VSS	AN22
BG17	VSS	VSS	P24	AD13	VSS	AN24
BG2	VSS	VSS	P25	AD15	VSS	AN25
BG22	VSS	VSS	P28	AD17	VSS	AN26
BG25	VSS	VSS	P38	AD18	VSS	AN31
BG28	VSS	VSS	P4	AD28	VSS	AN33
BG32	VSS	VSS	P45	AD38	VSS	AP12
BG37	VSS	VSS	P5	AD37	VSS	AP17
BG41	VSS	VSS	R21	AD45	VSS	AP21
BG9	VSS	VSS	R24	AD49	VSS	AP25
C1	VSS	VSS	R25	AD5	VSS	AP26
C12	VSS	VSS	R28	AD6	VSS	AP28
C24	VSS	VSS	T1	AD8	VSS	AP31
C4	VSS	VSS	T12	AD9	VSS	AP33
C49	VSS	VSS	T15	AE12	VSS	AP38
C7	VSS	VSS	T17	AE13	VSS	AP45
D1	VSS	VSS	T33	AE19	VSS	AP5
D13	VSS	VSS	T38	AE17	VSS	AT1
D2	VSS	VSS	T49	AE18	VSS	AT12
D25	VSS	VSS	T9	AE35	VSS	AT17
D3	VSS	VSS	U21	AE37	VSS	AT19
D35	VSS	VSS	U22	AE45	VSS	AT21
D43	VSS	VSS	U24	AE5	VSS	AT22
D44	VSS	VSS	U25	AE28	VSS	AT24
D48	VSS	VSS	U26	AG1	VSS	AT25
D49	VSS	VSS	U28	AG12	VSS	AT26
D7	VSS	VSS	U29	AG17	VSS	AT28
E1	VSS	VSS	U31	AG20	VSS	AT29
E15	VSS	VSS	U12	AG22	VSS	AT31
E19	VSS	VSS	U17	AG23	VSS	AT33
E24	VSS	VSS	U21	AG29	VSS	AT37
E28	VSS	VSS	U22	AG27	VSS	AT49
E29	VSS	VSS	U24	AG28	VSS	AT5
E26	VSS	VSS	U25	AG35	VSS	AL25
E31	VSS	VSS	U26	AG37	VSS	AL41
E33	VSS	VSS	U33	AG49	VSS	AV11
E35	VSS	VSS	V38	AH12	VSS	AV39
E37	VSS	VSS	W5	AH13	VSS	AV45
E39	VSS	VSS	W27	AH15	VSS	AV5
E9	VSS	VSS	W28	AH35	VSS	AW11
F25	VSS	VSS	W30	AH38	VSS	AW24
	VSS	VSS	W41			
	VSS	VSS	Y13			
	VSS	VSS	Y16			
	VSS	VSS	Y17			
	VSS	VSS	Y18			
	VSS	VSS	Y32			
	VSS	VSS	Y38			

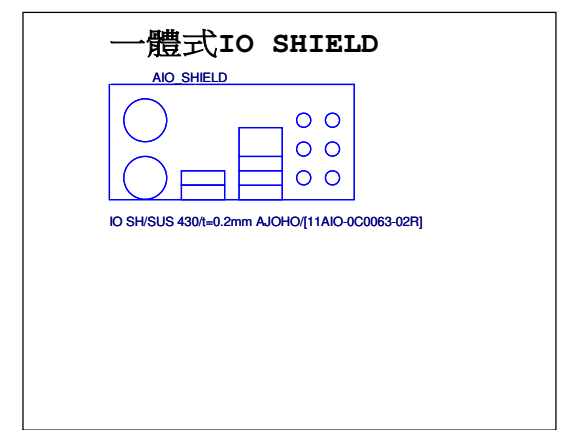
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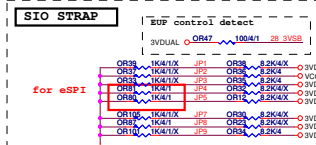
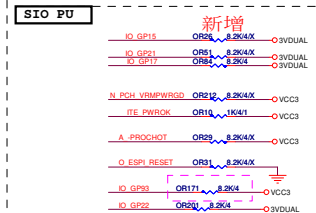
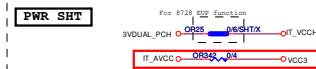
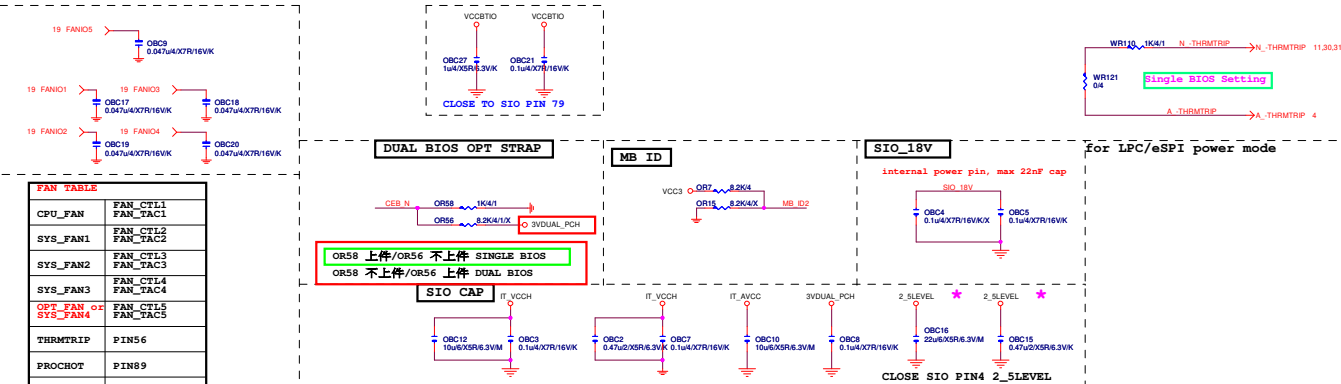
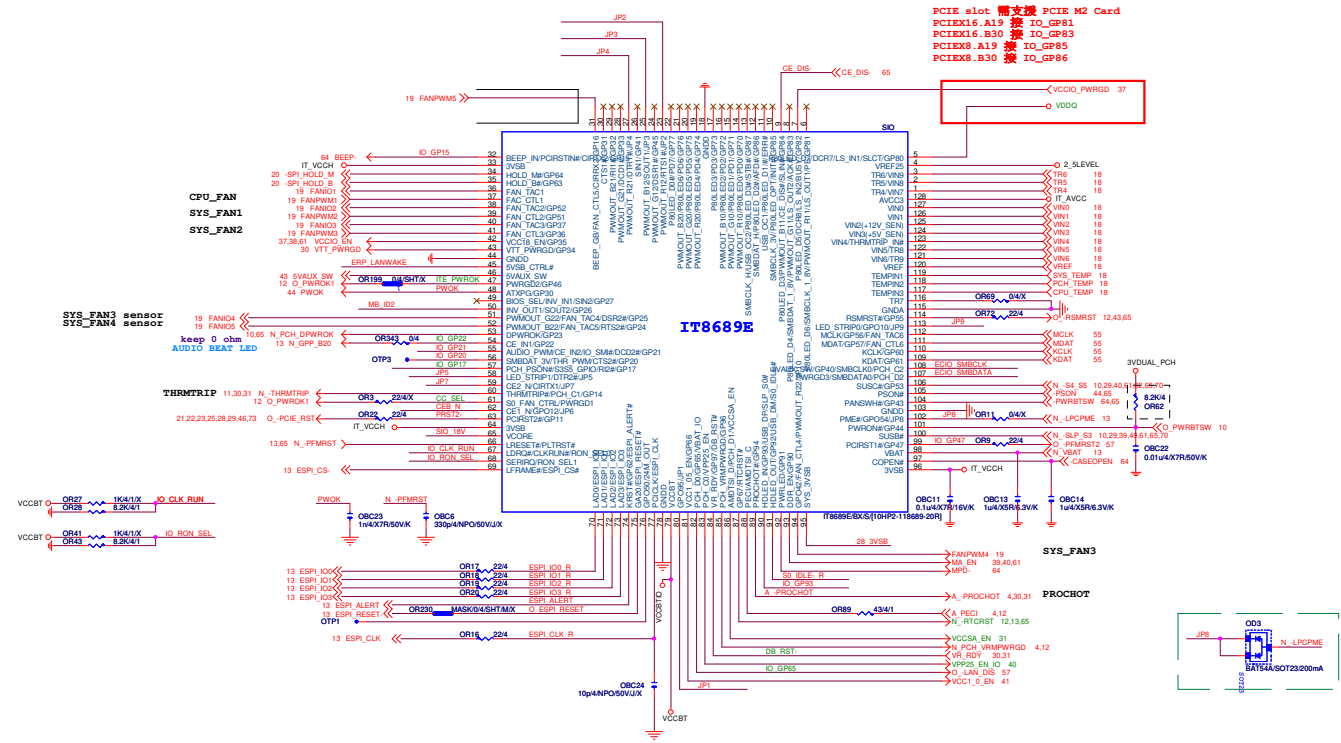
FH82B560/S[10H1-03B560-10F]

裝甲HEATSINK 分成四大部份

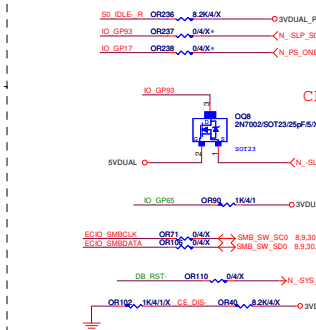


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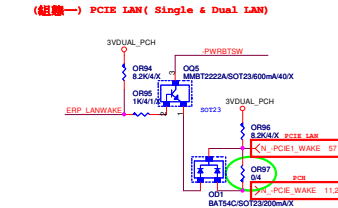




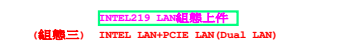
JP2	1	Disable WDT to reset PWROK
	0	Enable WDT to reset PWROK
JP3	1	Dual-BIOS CS pin mode select bit '0' See the below table
	0	
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for Gigabyte Only)
	0	Disable Dual BIOS Function (for Gigabyte Only)
JP7	1	Dual-BIOS CE pin mode select bit '1' See the below table
	0	
JP7	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
	0 1	CE mode 2
	0 0	CE mode 3



請依開案規格，選擇Support Erp下 LAN Wake up組態。



(組態二) INTEL219 LAN(Single LAN)



ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	
Dual LAN (只買一個 LAN 支援 WUE WAKE UP)	Intel 219	組態二
	Atheros+Atheros	組態一
	Intel 219+Atheros	
	Intel 219+Intel 210	組態三
No Support ERP	Single LAN BOM 只上 OR97 + Dual LAN BOM 只上 OR97 + OR99。	

<h1 style="text-align: center; color: blue;">Gigabyte Technology</h1>	
Title <div style="text-align: center;">IT8688</div>	
Size	Document Number <div style="text-align: center; font-size: 1.5em; font-weight: bold;">B560 AORUS PRO A</div>
Customer	Date: Thursday, February 25, 2021 <div style="float: right;"> Page 17 of 7 </div>

Figure 1: Schematic diagram of the temperature sensor circuit. The circuit shows four temperature inputs: VREF, SYS_TEMP, CPU_TEMP, and PCH_TEMP. Each input is connected to a voltage divider network. VREF is connected to a 10K/4/1 resistor (OR73) and a 8.2K/4 resistor (R674). SYS_TEMP is connected to a 10K/1/4/5 resistor (SYS_TEMP1) and a 10K/4/1 resistor (R675). CPU_TEMP is connected to a 10K/1/4/5 resistor (SYS_TEMP1) and a 10K/4/1 resistor (R675). PCH_TEMP is connected to a 10K/1/4/5 resistor (PCH_TEMP) and a 10K/4/1 resistor (R675). The circuit also includes a 1u/4X5R6.3V/K capacitor (OC7) and a 1u/4X5R6.3V/K capacitor (OC6). The circuit is labeled with 'Close S10' and 'CLOSE PCH'.

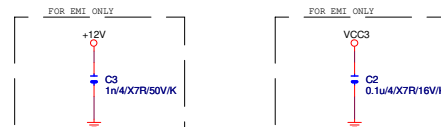
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VCC_SIO V

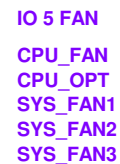
OR82

0/4/SHT/X

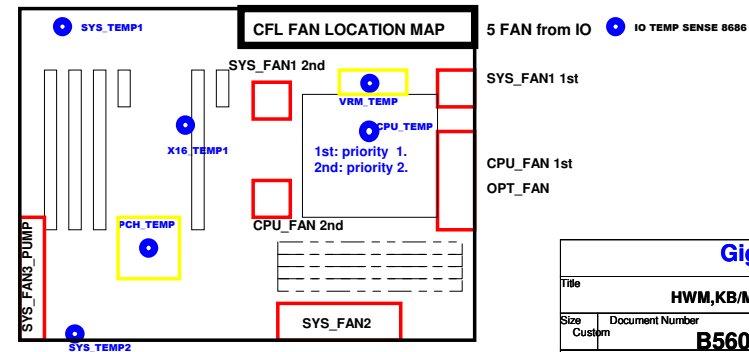
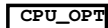
Rev:0.6



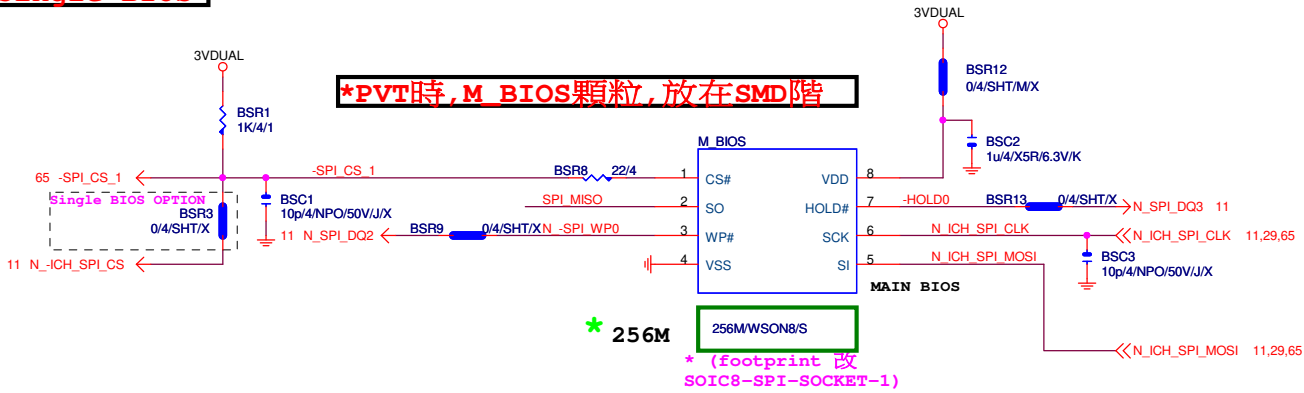
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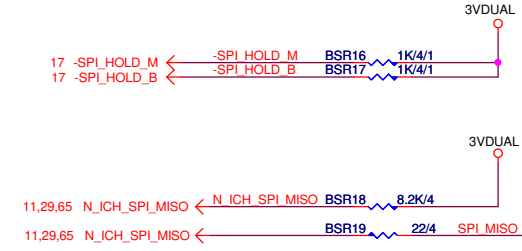
SYSTEM FAN1



DUAL BIOS *Single BIOS



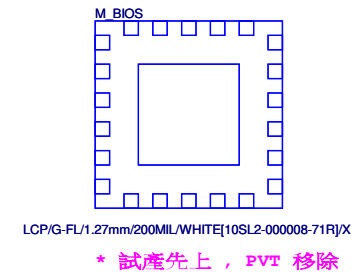
MOSI For DMI RX Termination Voltage



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BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

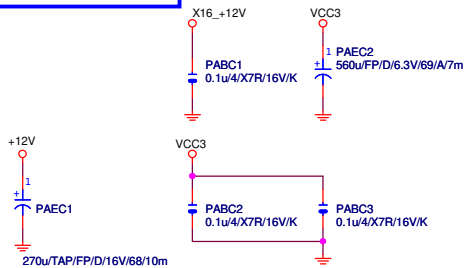


Rev 0.3

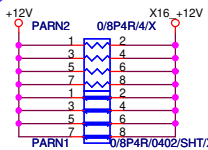
PCIEX16 CAP

PCIEX16 SLOT

PCIESLOT-1645TH



PCIEX16 PROTECT SHT

+12 protect
short-wire test

PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP TXN15 C

PCI-E REV:1.1--> 2.5GHz

PCE-E X1(單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz*(8b/10b) X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b) X16=32Gb/s=4GB/s

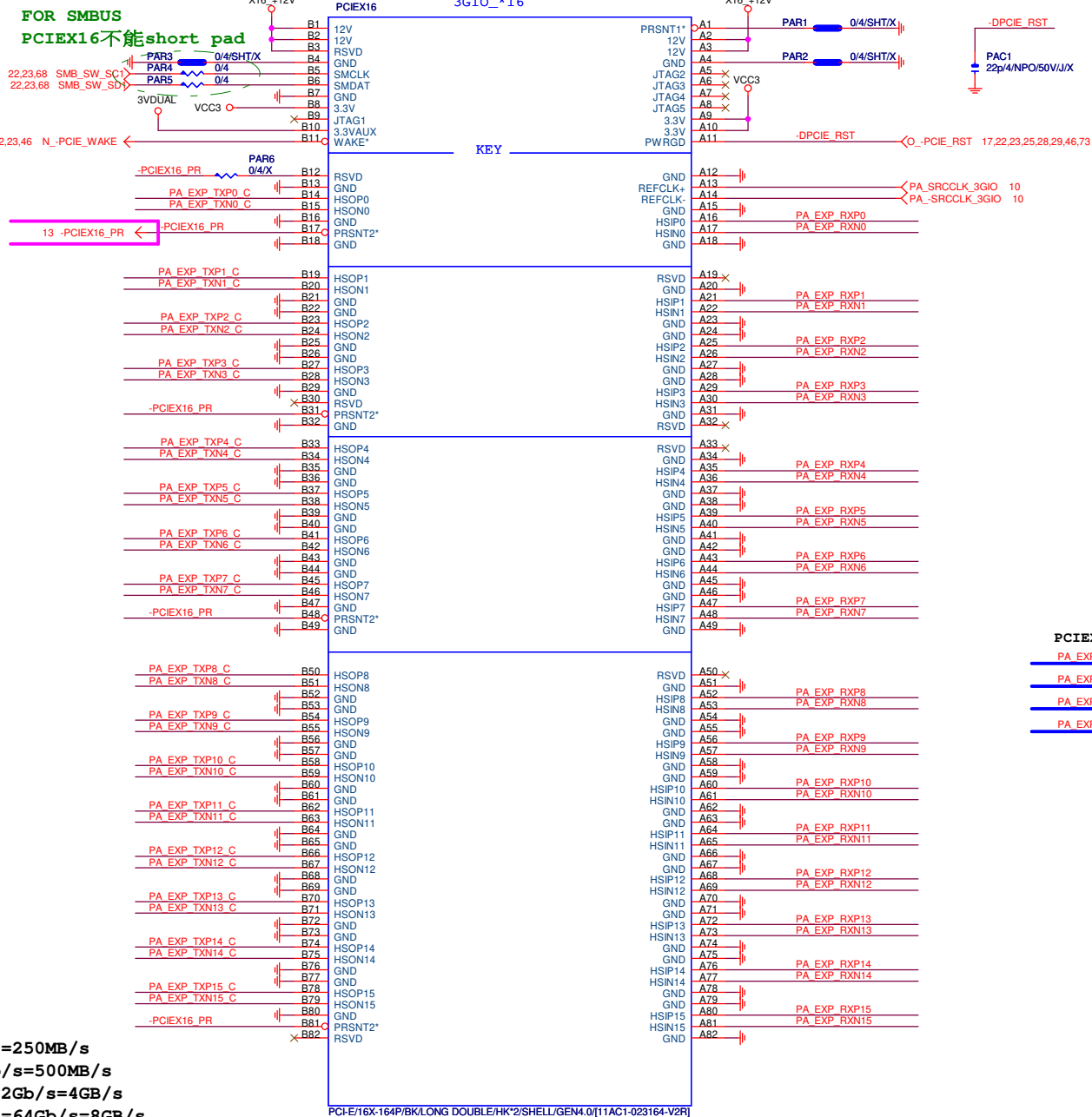
PCE-E X16(雙向) BANDWIDTH=2.5GHz*(8b/10b) X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHz

PCE-E X1(單向) BANDWIDTH=5GHz*(8b/10b)=4Gb/s=500MB/s

PCI-E REV:3.0--> 8GHz

PCE-E X1(單向) BANDWIDTH=8GHz*(128b/130b)=8Gb/s=1GB/s



PCI-E16X-164P/BK/LONG DOUBLE/HK*2/SHELL/GEN4.0[11AC1-023164-V2R]

黑色 金屬加強

PCIEX16:16/5/5/5/16

PA EXP RXP[0..15] >>> PA_EXP_RXP[0..15] 4
PA EXP RXN[0..15] >>> PA_EXP_RXN[0..15] 4
PA EXP TXP[0..15] >>> PA_EXP_TXP[0..15] 4
PA EXP TXN[0..15] >>> PA_EXP_TXN[0..15] 4

Gigabyte Technology

Title			PCI EXPRESS * 16
Size	Document Number	B560 AORUS PRO AX	
Custom			Rev 1.02
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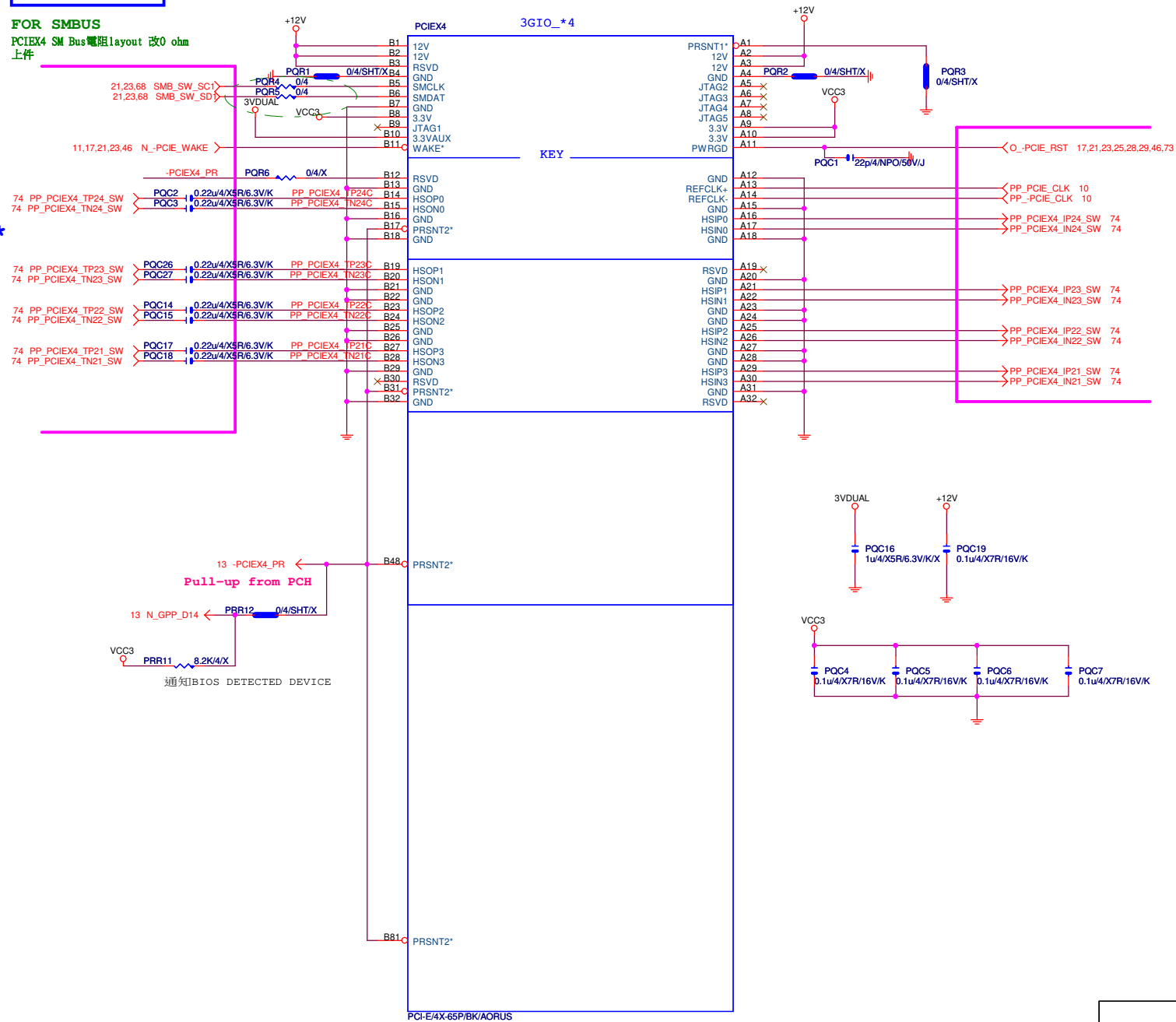
Rev 0.51

PCIE*4

* Footprint "PCIESLOT-64STH-1"

FOR SMBUS

PCIEX4 SM Bus電阻layout 改0 ohm
上件



黑色

Gigabyte Technology

Title			
PCIE X4			
Size Custom	Document Number		Rev
	B560 AORUS PRO AX		1.02
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PCIE_X4

B560 AORUS PRO AX

1.02

PCIEX1

PCIEX1

3GIO_*4

PRSENT1*
12V

KEY

KEY _

PCI-E/4X-65P/BK/AORUS

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PCIE X1 *3

B560 AORUS PRO AX

1.02

Date: Thursday, February 25, 2021 Sheet 23 of 74

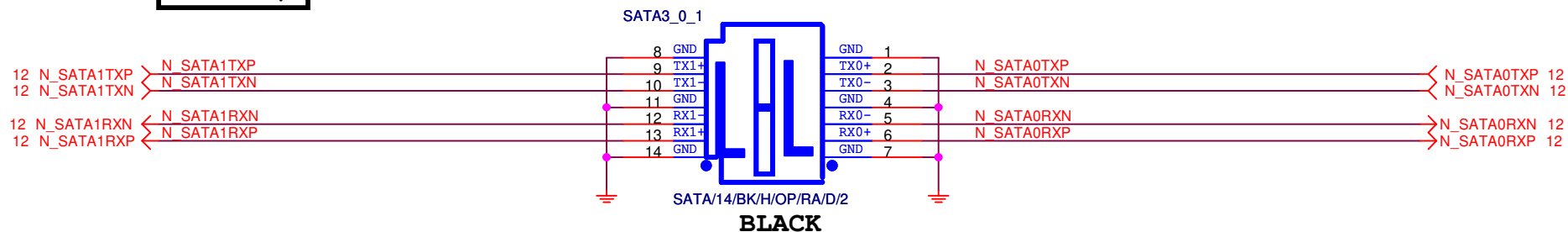
IO18/IO19 To SATA3 port0/1

6 SATA3 from Z490 (90度R-A)

SATA3 0/1

上 Port (8~14)

下 Port (1~7)

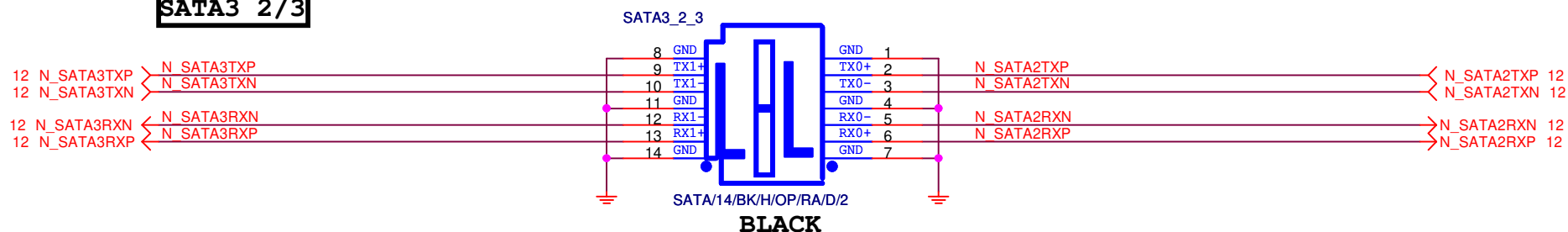


Footprint : H2X7-SATA2-D90

IO20/IO21 To SATA3 port2/3

上 Port (8~14)

下 Port (1~7)

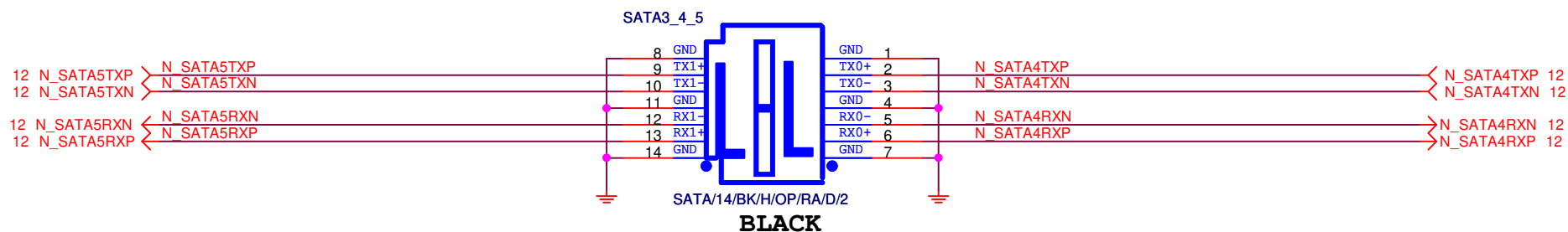


Footprint : H2X7-SATA2-D90

IO22/IO23 To SATA3 port4/5

上 Port (8~14)

下 Port (1~7)



Footprint : H2X7-SATA2-D90

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Title

SATA

Size
Custom

Document Number

B560 AORUS PRO AX

Rev

1.02

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M.2 Lane4 from PCH port9

M.2 Lane3 from PCH port10

M.2 Lane2 from PCH port11

M.2 Lane1 from PCH port12

支援SATA and M.2 function

REVERSED

SATA : GND.

PCIE : NC

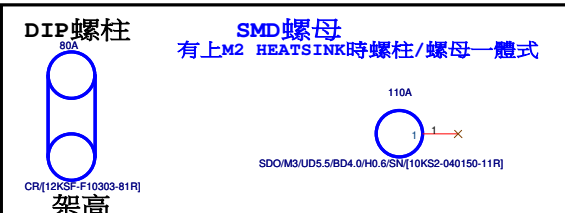
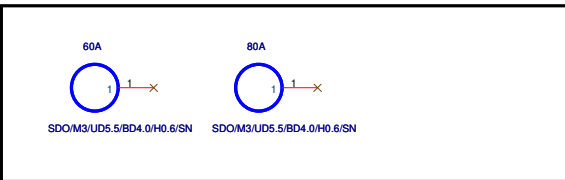
M2插卡時為Low

架高

Footprint : M2_110_H2MM8W

Flex IO priority	N_GPP_K1	IO14 PCIe#9	IO15 PCIe#10	IO16 PCIe#11	IO17 PCIe#12
M2A SATA	L	PCIE	PCIE	SATA 0	SATA 1
M2A PCIE (PCIE Reverse)	H	PCIE	PCIE	PCIE	PCIE

可變動



有上M2 HEATSINK時特制螺絲



Gigabyte Technology

Title		
M.2 X4		
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Rev 0.1

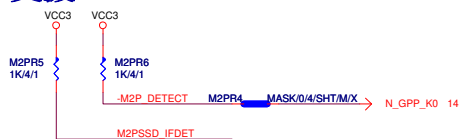
M.2 Lane4 from CPU port4

M.2 Lane3 from CPU port3

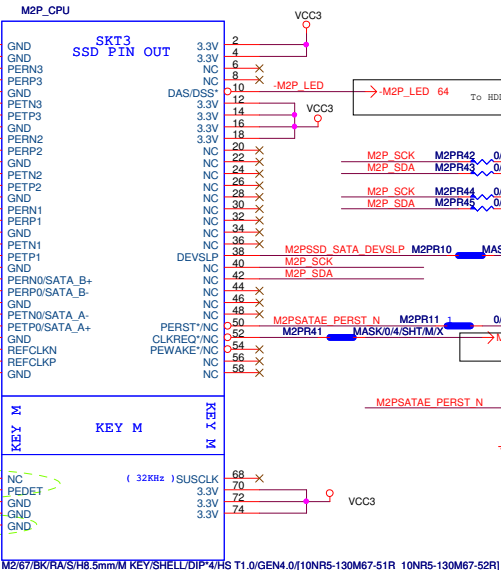
M.2 Lane2 from CPU port2

M.2 Lane1 from CPU port1

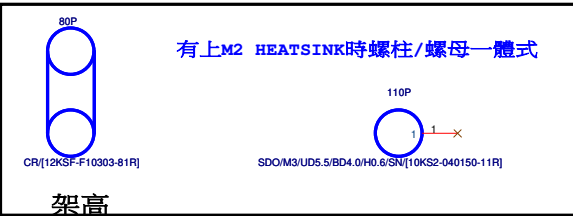
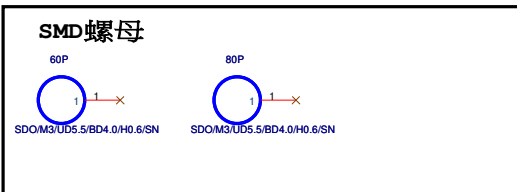
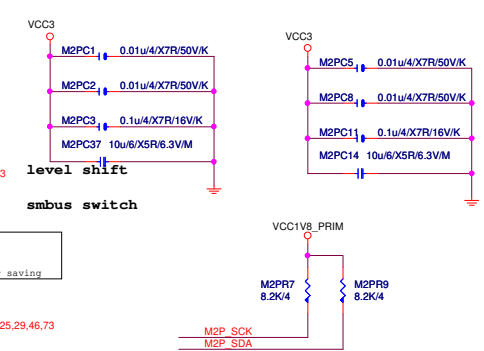
支援SATA and M.2 function



需與M2_-CLKREQ對應



Footprint : M2_110_H2MM8W

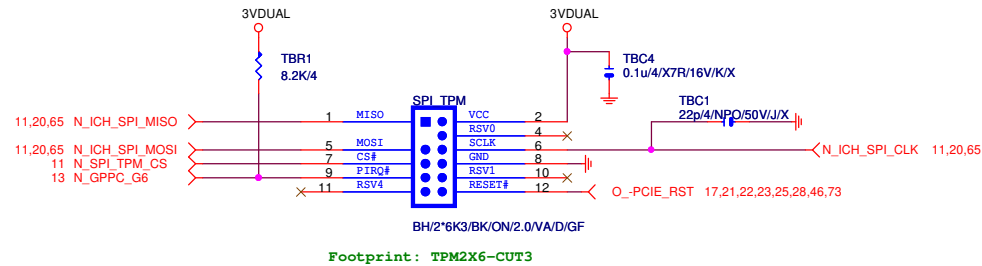


M2P_CPU_HS
M2 HEATSINK
M2P_CPU_HS[12SP1-S13905-32R_12SP1-S13905-34R_12SP1-S13905-35R]:M2P_CPU_HS

RTD3 GPIO refer by Intel RVP

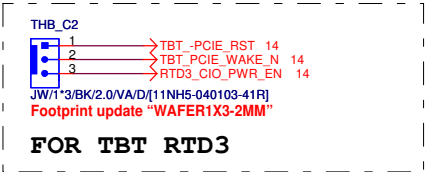
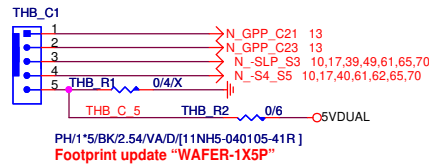
GPIO	CFL-S	CML-U	CML-H	CML-S
TBT_PERST_N	GPP_F_2	GPPC_C15_SLOT1_RST_N	GPP_F4_SATAPCIE7	GPP_F2
TBT_Wake_N	GPP_H_15	GPPC_D11_SLOT1_WAKE_N	GPPK_18	GPP_H15
RTD3_PWN_EN	GPP_I_5	GPPC_D15	GPP_H_16_SML4_CLK	GPP_K23

TPM CONNECT



Thunderbolt

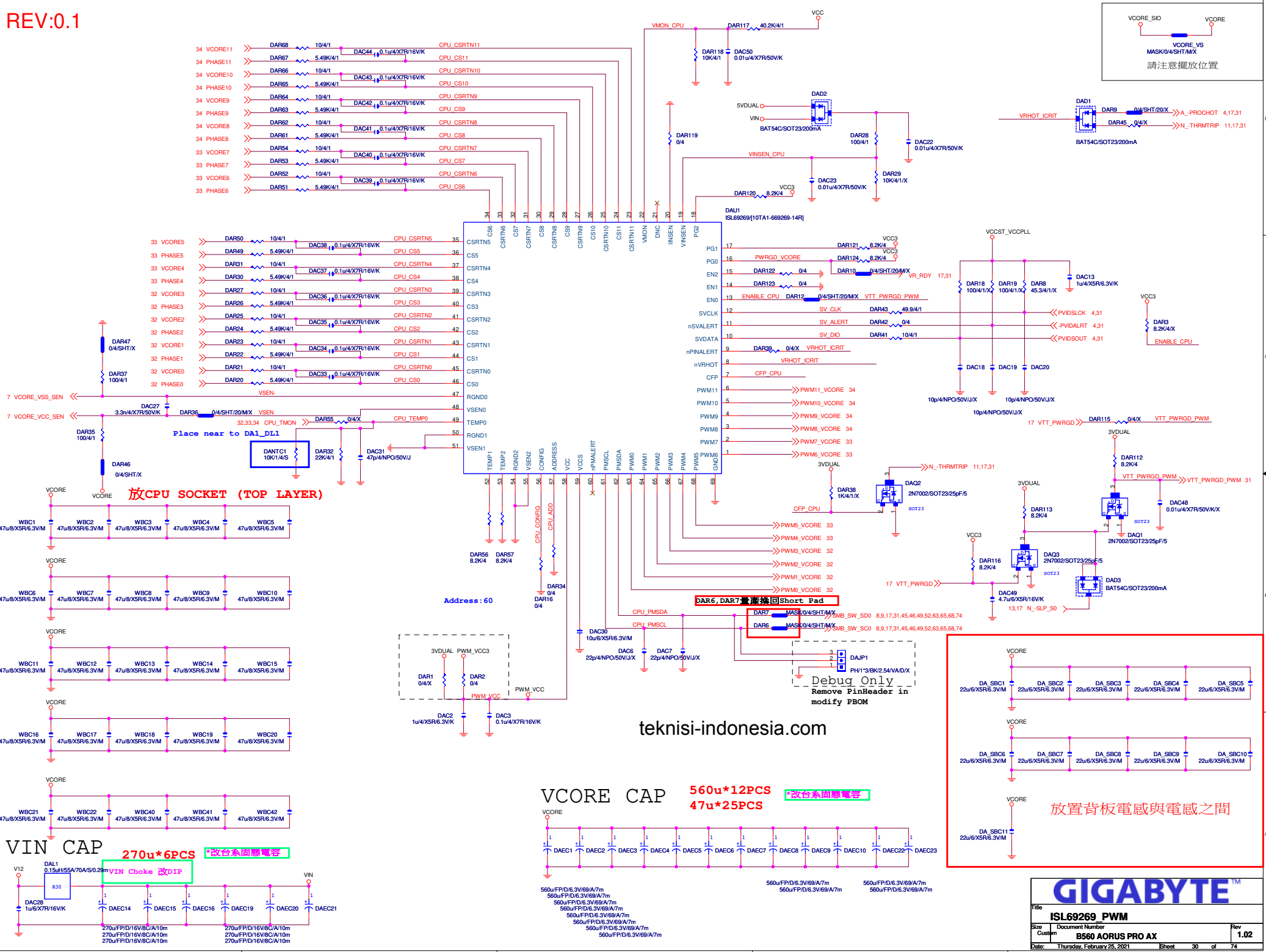
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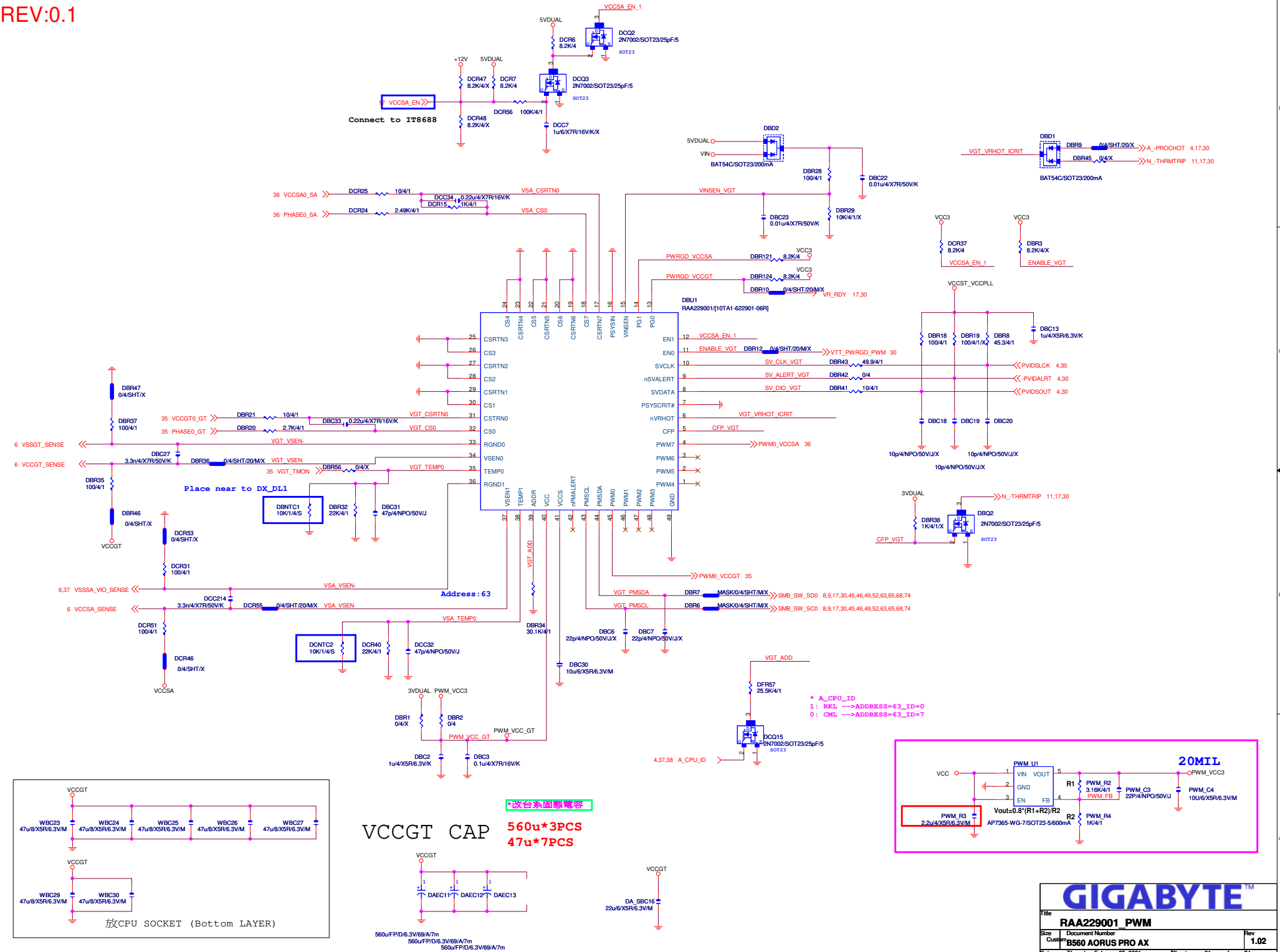


Z490系列使用

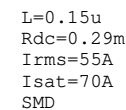
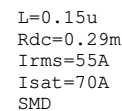
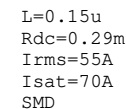
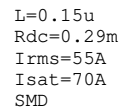
TBT_-PCIE_RST : CFL connector to GPP_F_2
TBT_PCIE_WAKE_N : CFL connector to GPP_H_15
RTD3_CIO_PWR_EN : CFL connector to GPP_K_23

REV:0.1



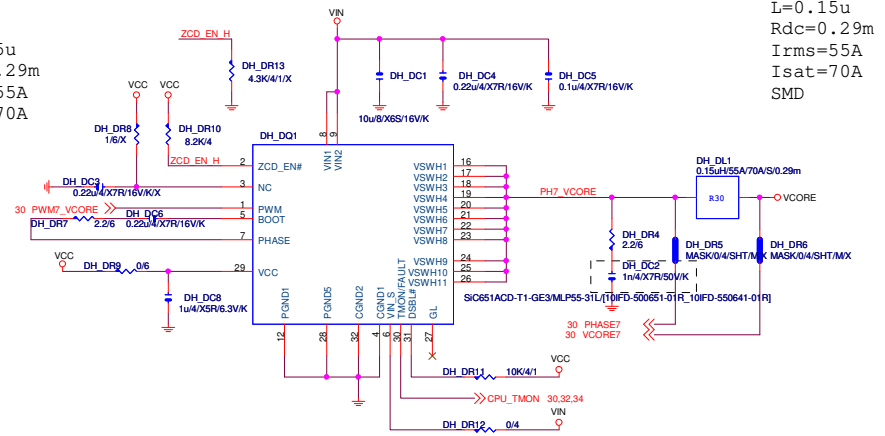
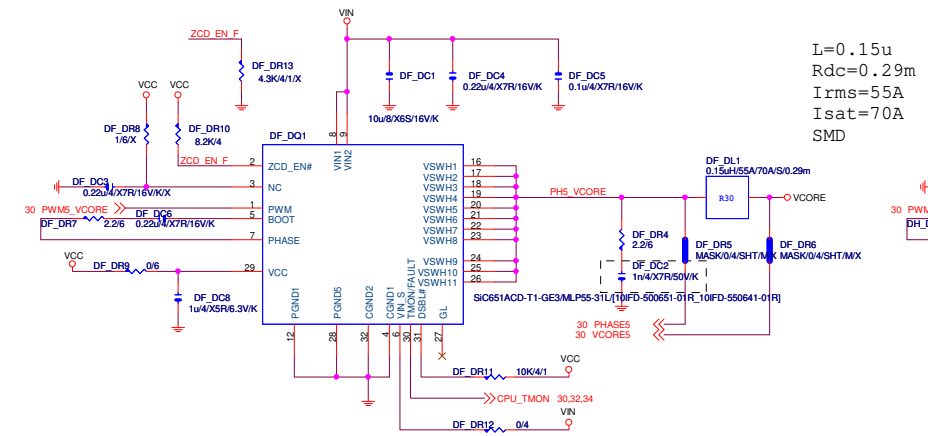
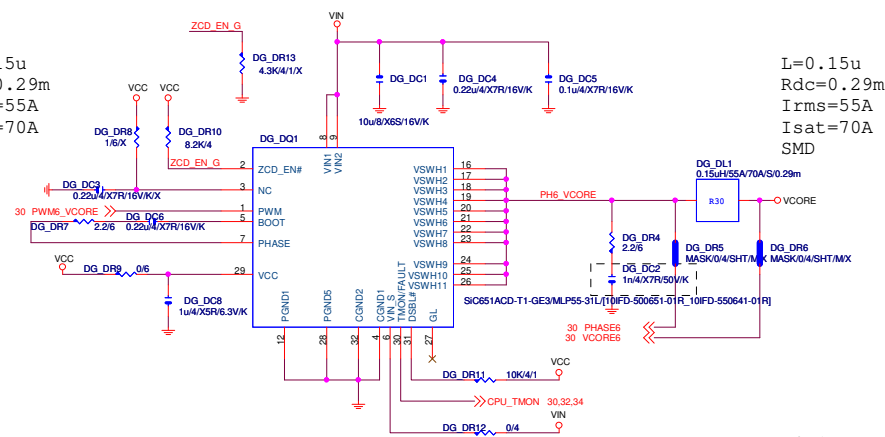
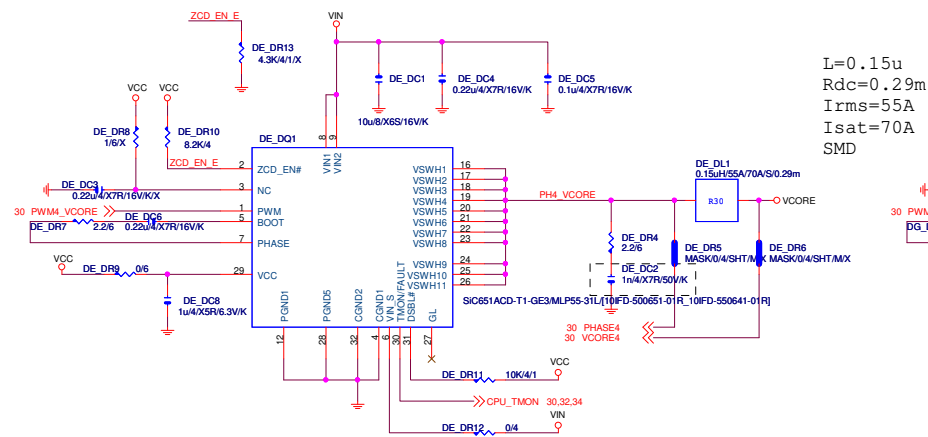


DRMOS使用NCP302155時PIN2 and PIN3要上件(Ex:DA_DR13.DA_DR8.DA_DC3)



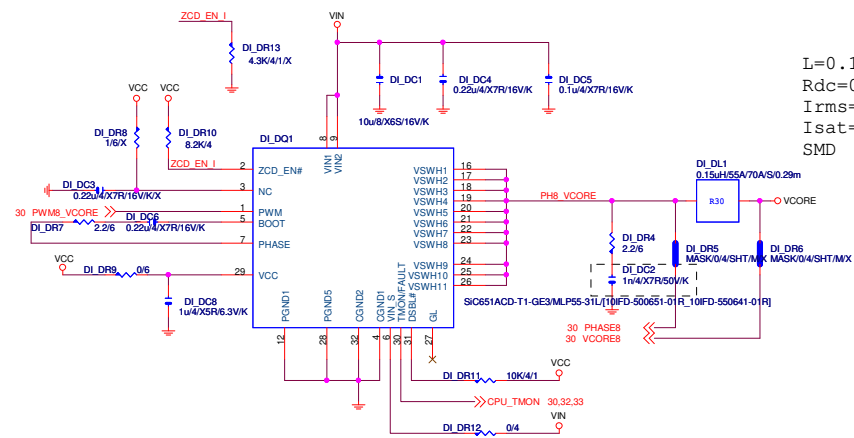
REV:0.1

DRMOS使用NCP302155時PIN2 and PIN3要上件(Ex:DA_DR13.DA_DR8.DA_DC3)

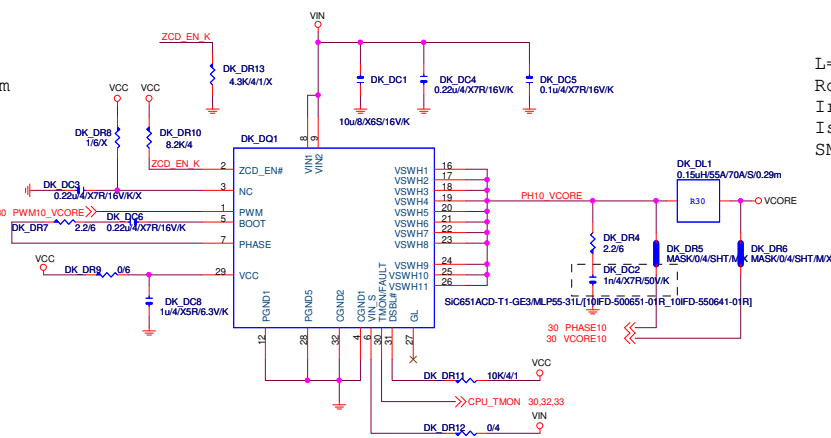


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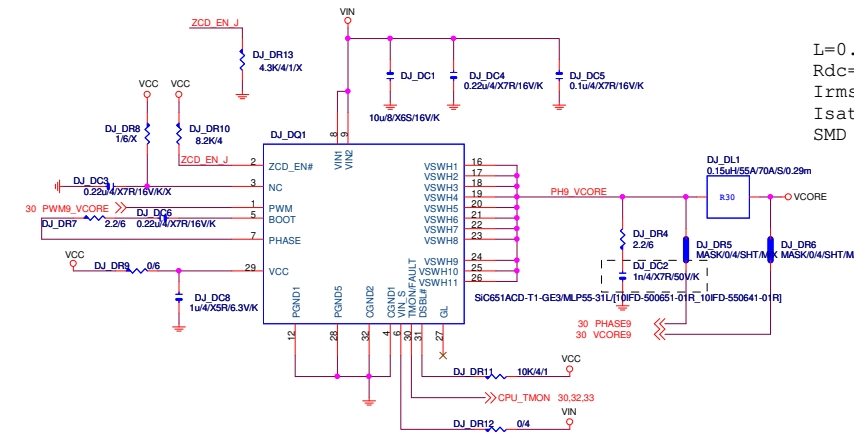
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Size	Document Number	Rev	1.02
Custom	B560 AORUS PRO AX		
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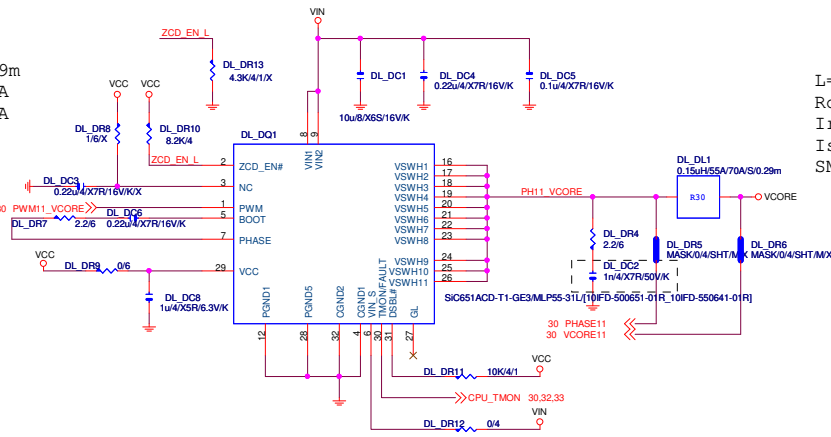
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



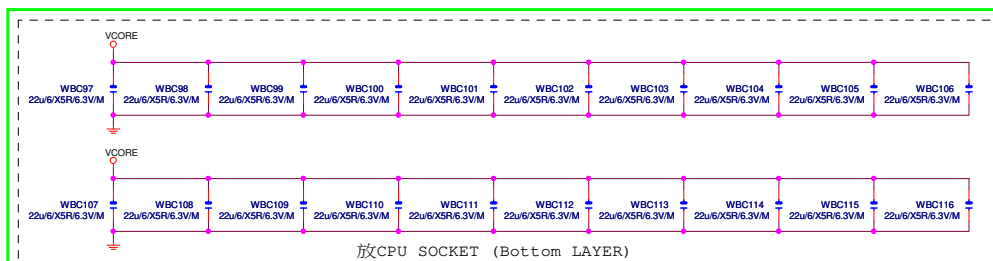
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



放CPU SOCKET (Bottom LAYER)

放CPU SOCKET (Bottom LAYER)

*Del SPCAP

*Del SPCAP

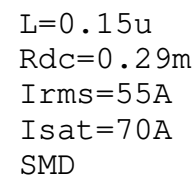
請版主自行確認是否使用
請版主自行確認使用330u or 470u

請版主自行確認使用組態

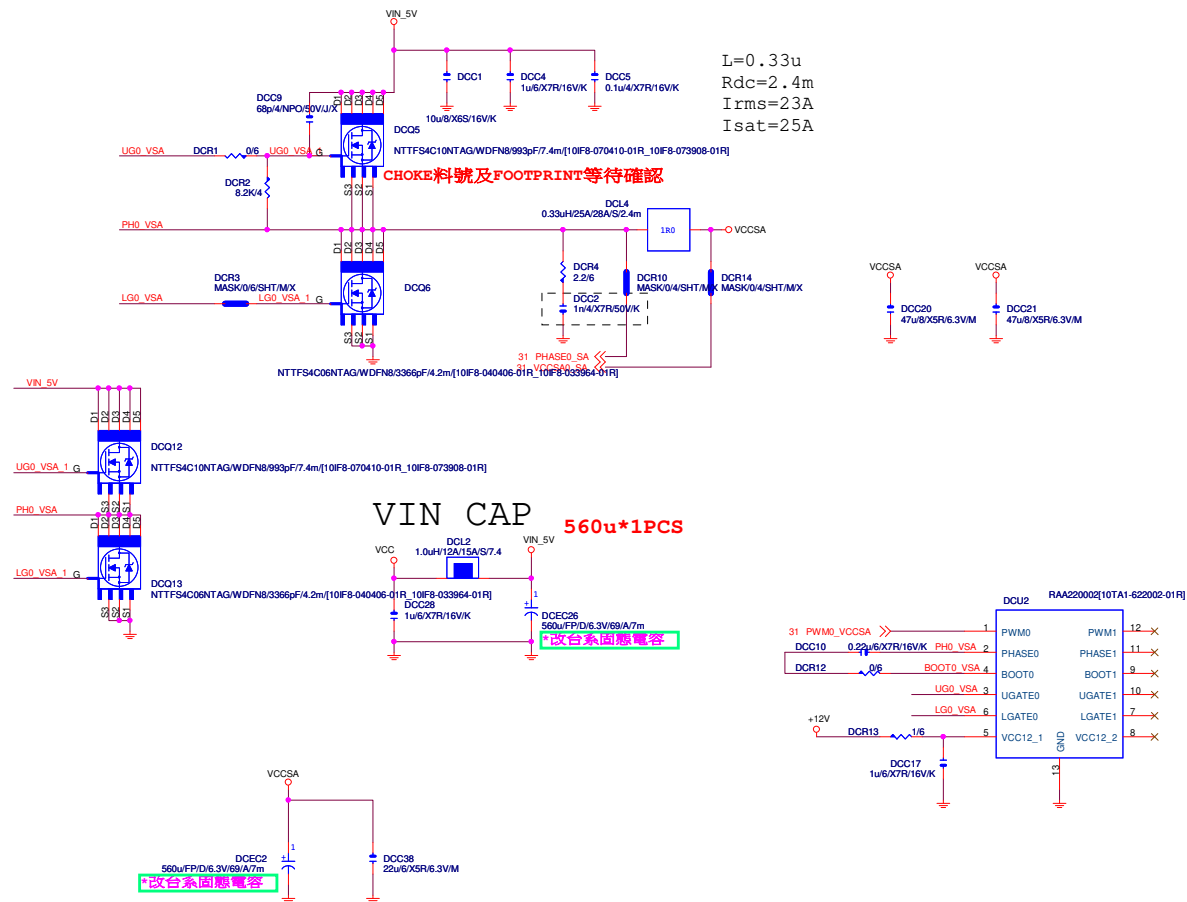
GIGABYTE™

Title			VCORE DRMOS-3
Size	Document Number	Rev	1.02
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DRMOS使用NCP302155時PIN2 and PIN3要上件(Ex:DA_DR13.DA_DR8.DA_DC3)

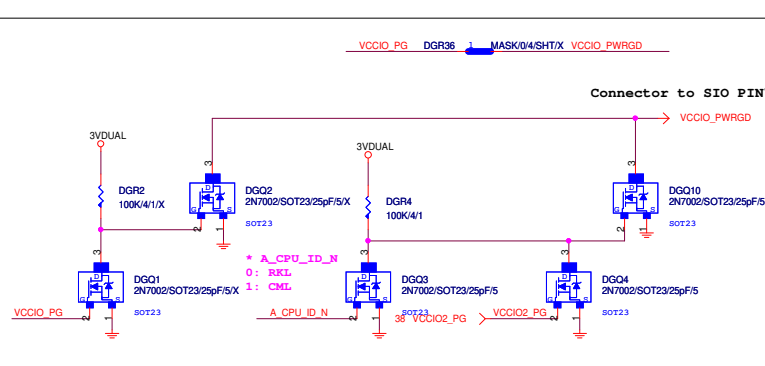
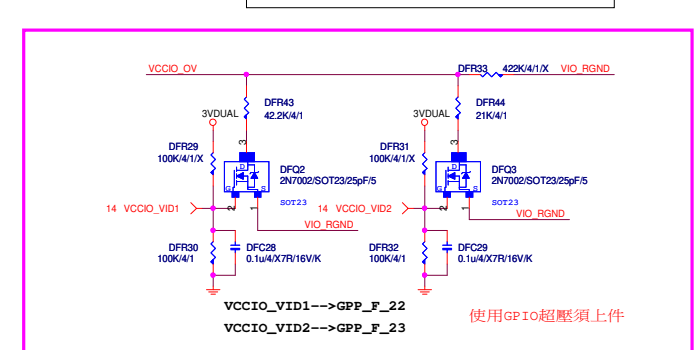
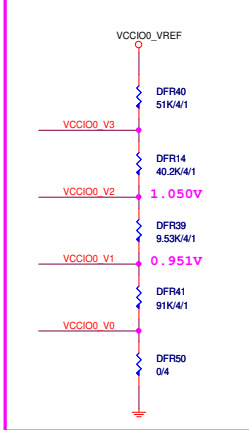
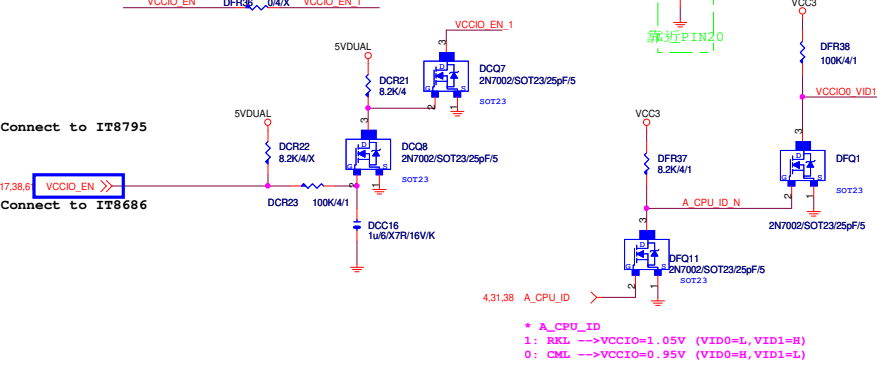
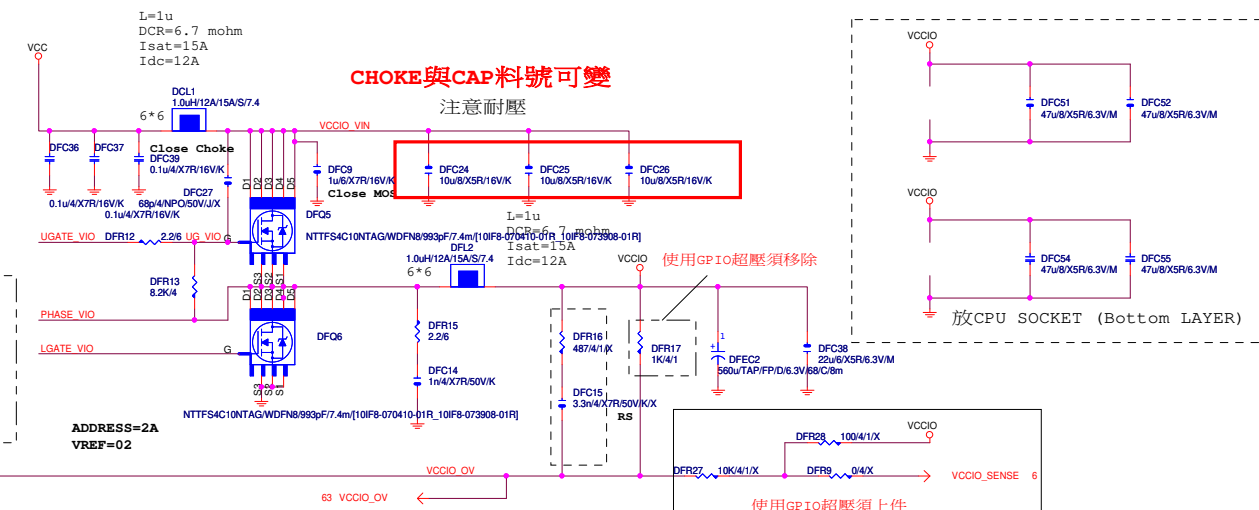
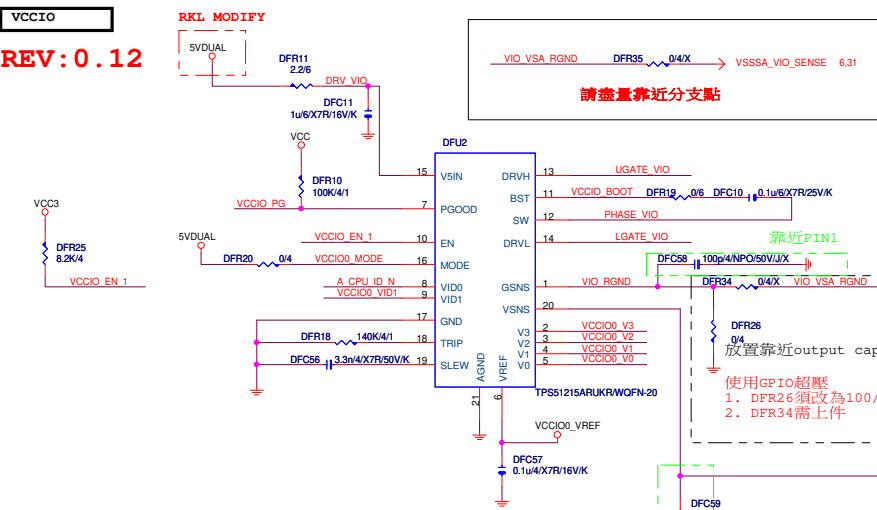


REV:0.1



CPU SOCKET 已經有22u/6 *4pcs

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VCCIO_VID1	VCCIO_VID2	VCCIO_0_G1	VOUT
LOW	LOW	LOW	0.950V
LOW	LOW	HIGH	1.050V
HIGH	LOW	HIGH	1.075V
LOW	HIGH	HIGH	1.100V
HIGH	HIGH	HIGH	1.125V

Mode	VR	Mode logic	LPM	VID Setting		Vout (V)
				G1 logic	G0 logic	
Mode1	VCCIO	0	0	x	x	0(LPM)
			1	0	0	0.85
			1	0	1	0.875
			1	1	0	0.95
			1	1	1	0.975
Mode2	VPRIMCORE	Floating	0	x	x	0.7V(LPM)
			1	0	0	0.85
			1	0	1	0.9
			1	1	0	0.95
			1	1	1	1
Mode3	VccEDRAM/ VccEOPIO	1	0	x	x	0(LPM)
			1	0	0	0.8
			1	0	1	0.95
			1	1	0	1
			1	1	1	1.05

GIGABYTE

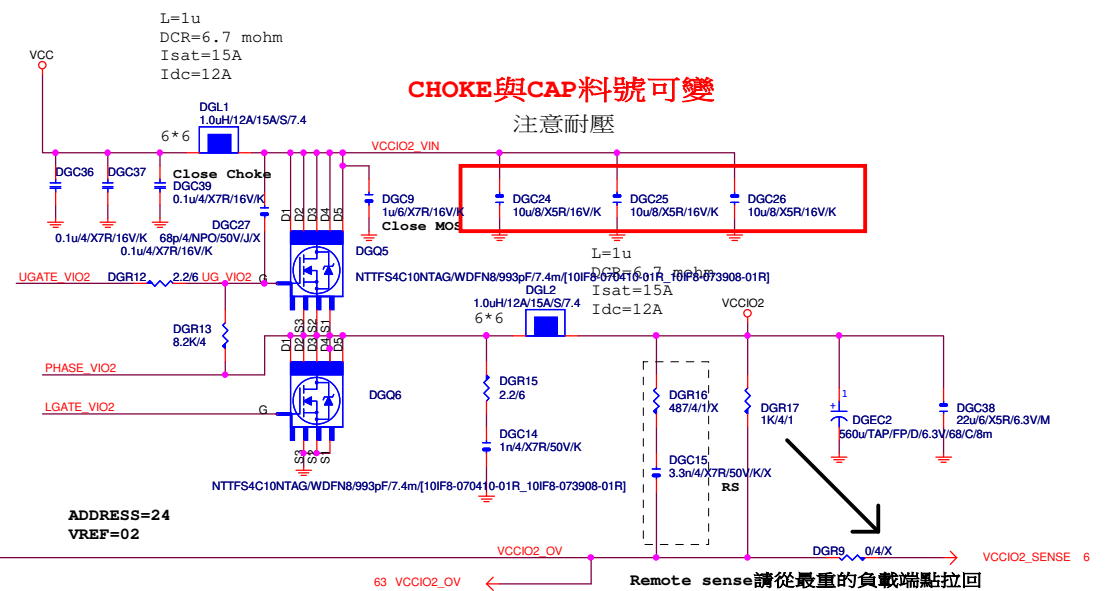
File **VCCIO**

Size Custom Document Number **B560 AORUS PRO AX** Rev **1.02**

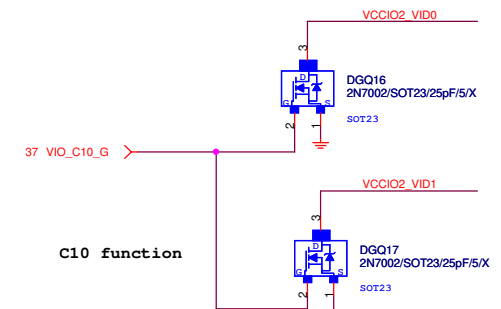
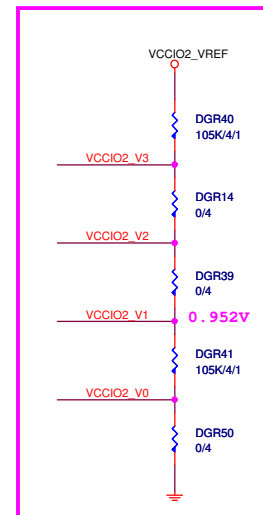
Date: Thursday, February 25, 2021 Sheet 37 of 74

RKL MODIFY

5VDUAL



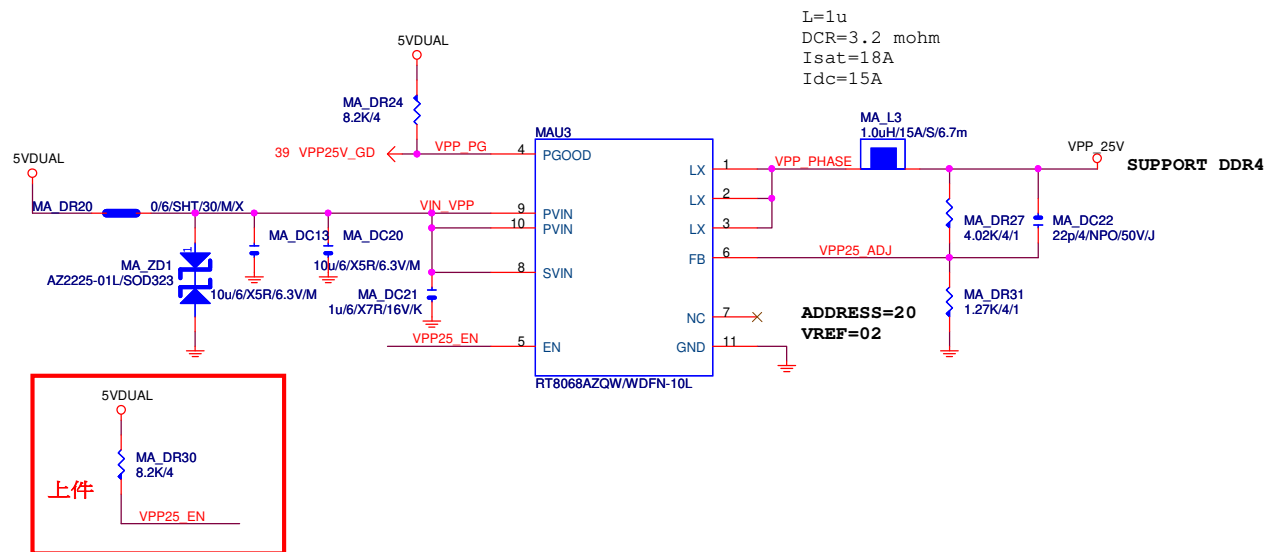
4,31,37 A_CPU_ID >



REV:0.1

VPP 25V

CHOKE與CAP料號可變

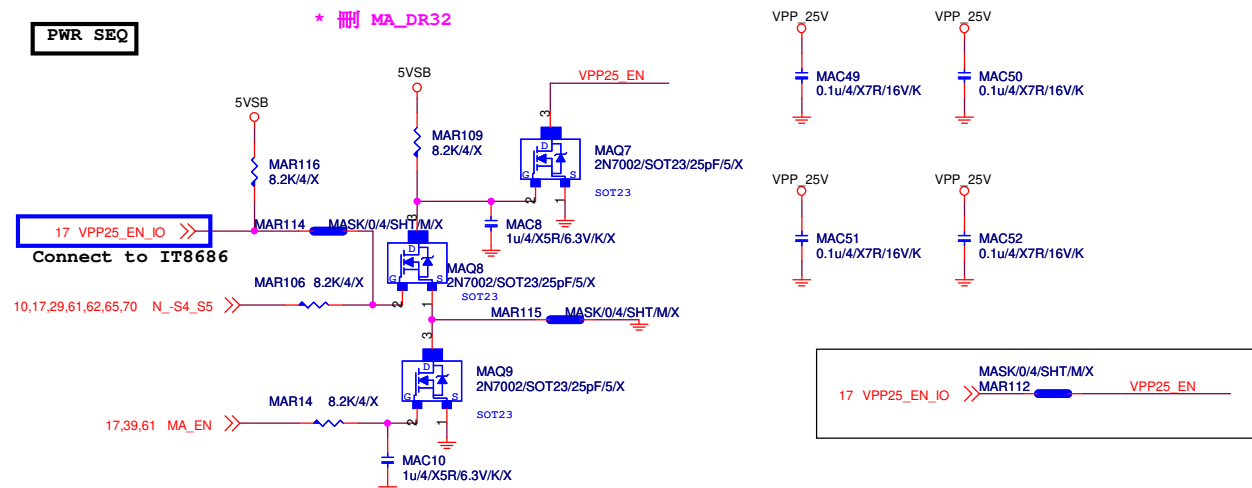


請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件

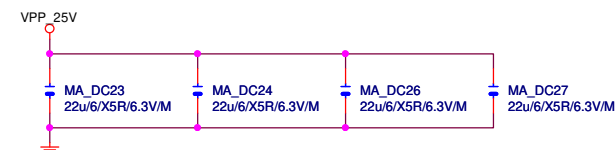
teknisi-indonesia.com

PWR SEQ

* 刪 MA_DR32



VPP CAP 22u*4PCS

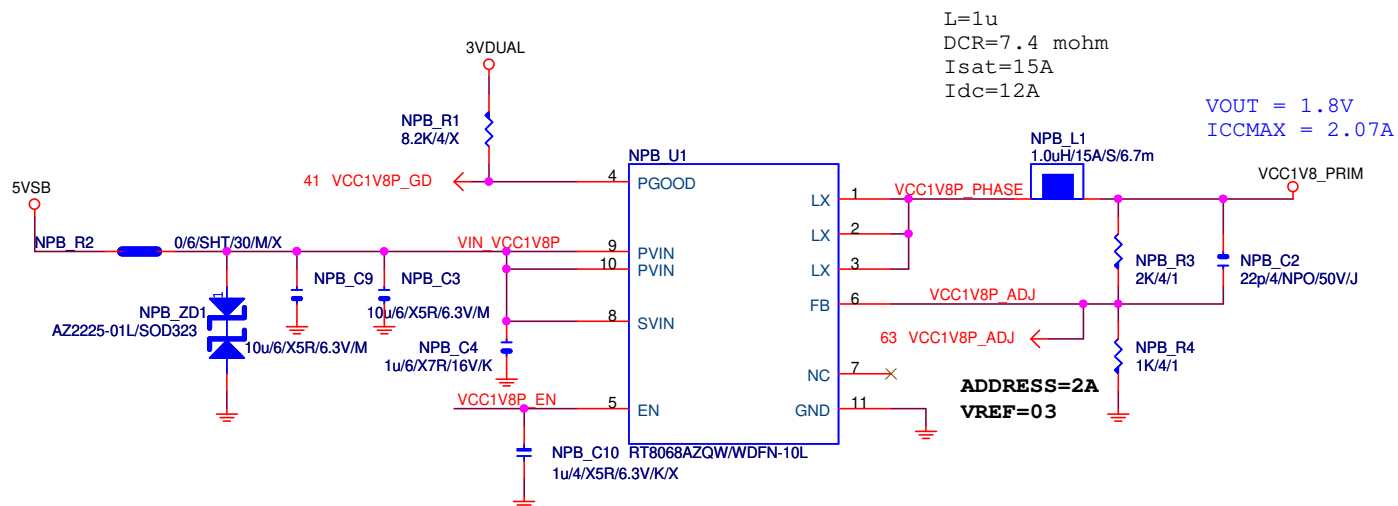


GIGABYTE™

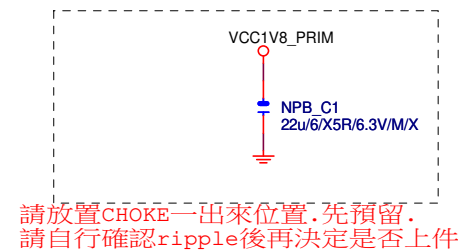
Title		
RT8068_VPP25 POWER		
Size	Document Number	Rev
Custom	B560 AORUS PRO AX	1.02
Date:	Thursday, February 25, 2021	Sheet 40 of 74

REV:0.1

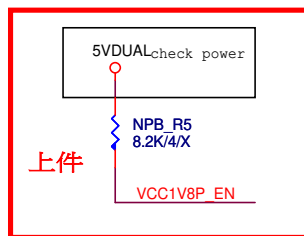
VCC1V8 PRIM



CHOKE與CAP料號可變



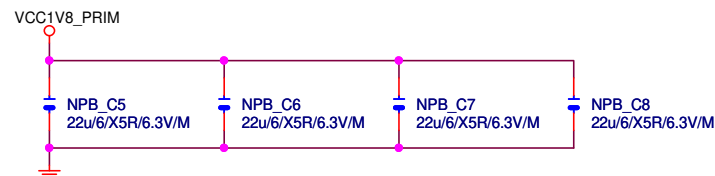
PWR SEQ



connect to PCH pin AD46

11,41 SLP_SUS_N >> NPB_R6 0/4 VCC1V8P_EN

VCC1V8_PRIM CAP 22u*4PCS



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Title
RT8068_VCC1V8_PRIM

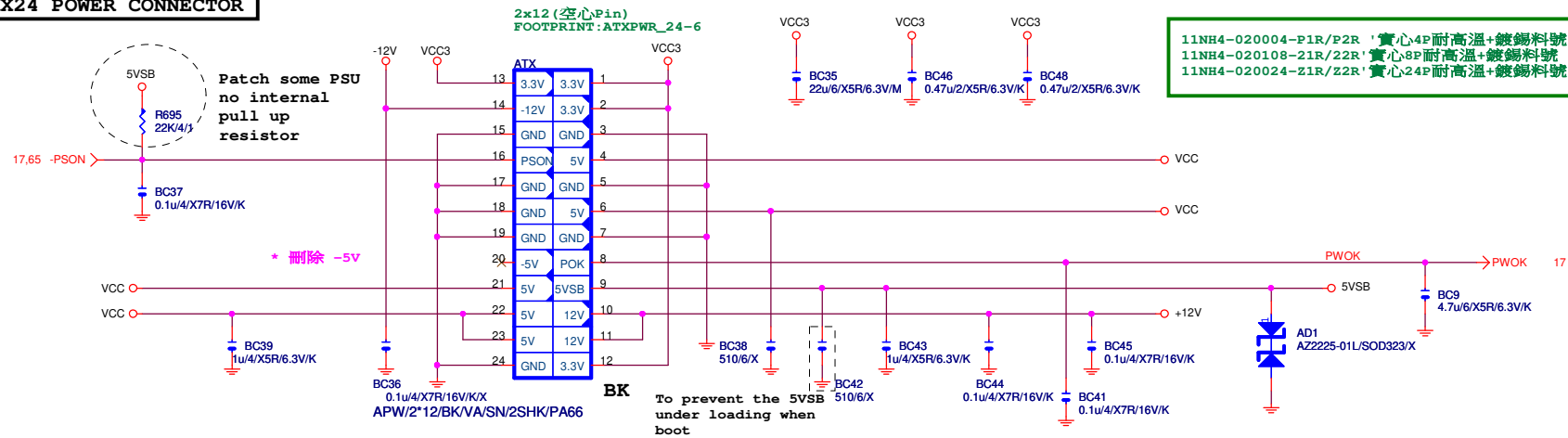
Size Custom Document Number
B560 AORUS PRO AX

Date: Thursday, February 25, 2021

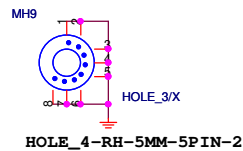
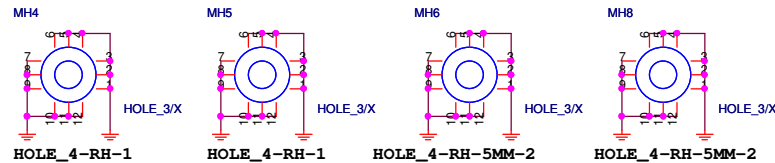
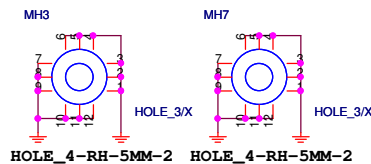
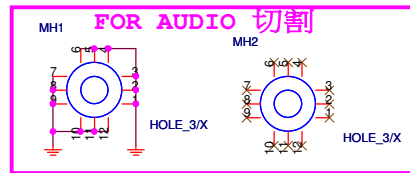
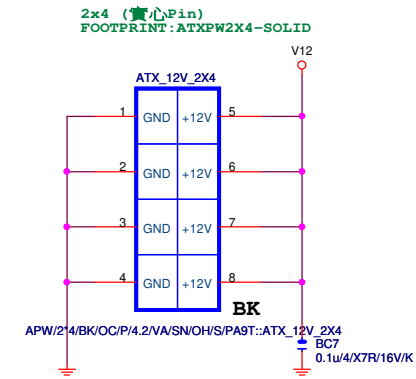
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Rev
1.02

ATXX24 POWER CONNECTOR

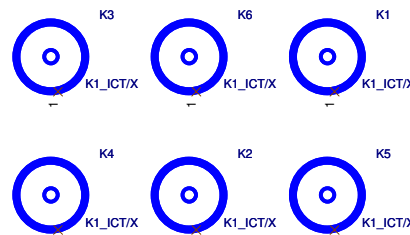


ATXX4 POWER CONNECTOR



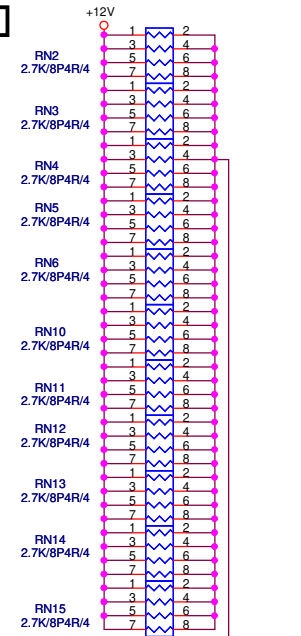
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固定孔/光學點

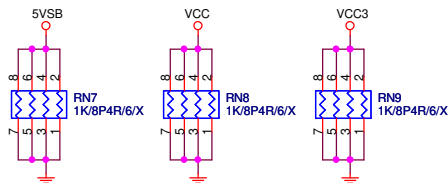


+12V DUMMY LOAD

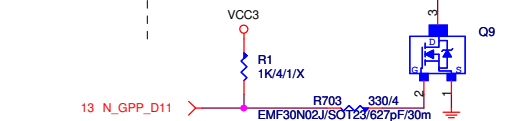
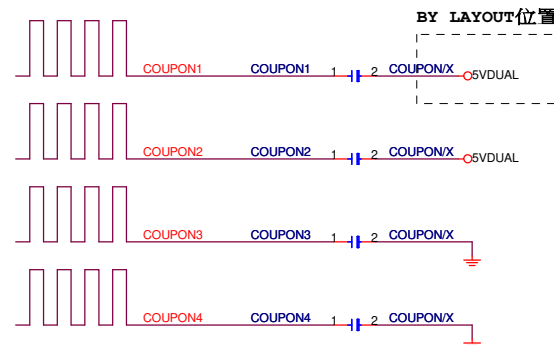
To fix 12V light load
abnromal issue



DUMMY LOAD



COUPON

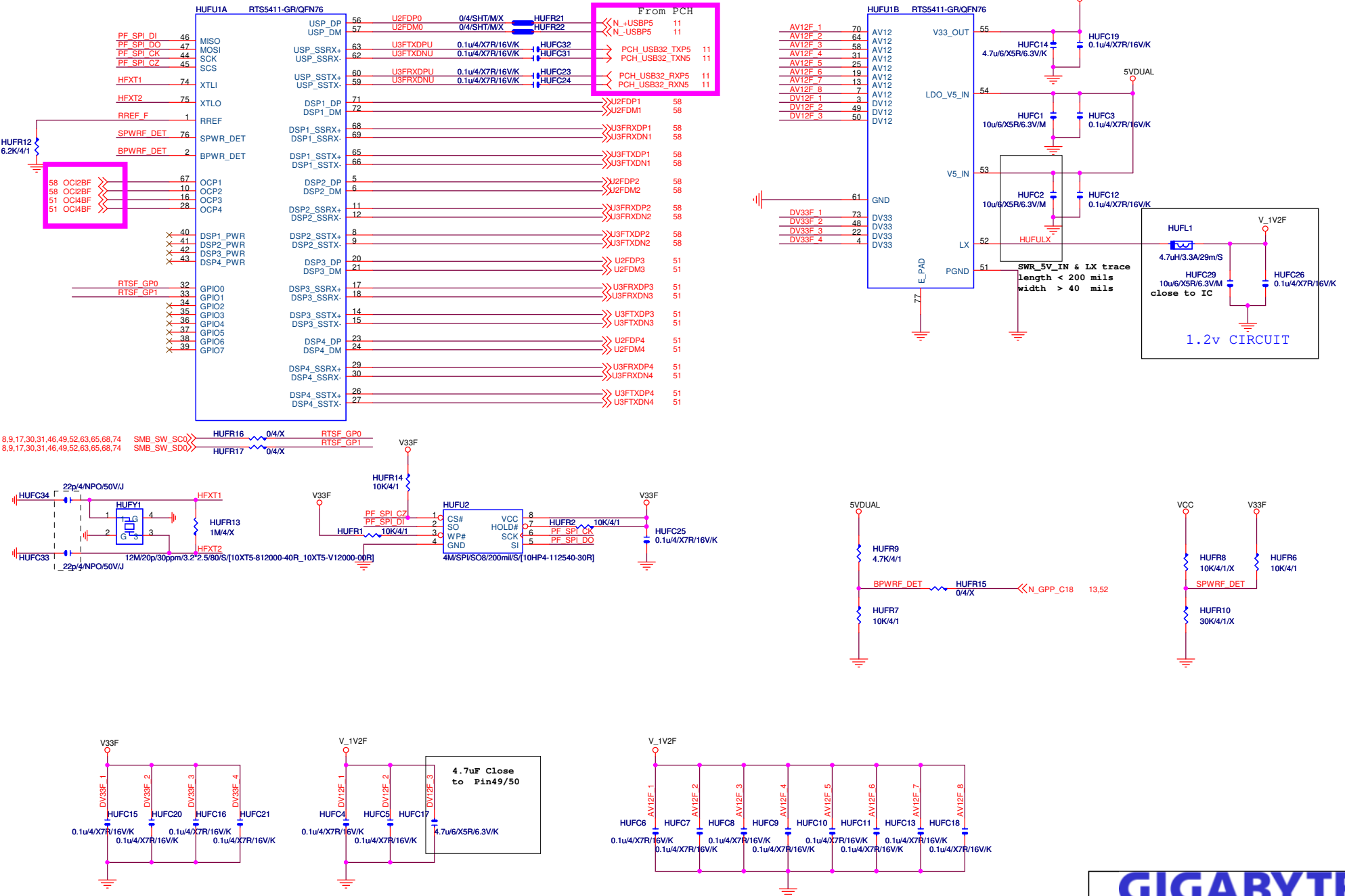


Gigabyte Technology

Title			ATX POWER CONNECTOR	
Size	Custom	Document Number	B560 AORUS PRO AX	
Date:	Thursday, February 25, 2021	Sheet	44	of 74
			1	Rev 1.02

RTS5411 HUB Rev0.1

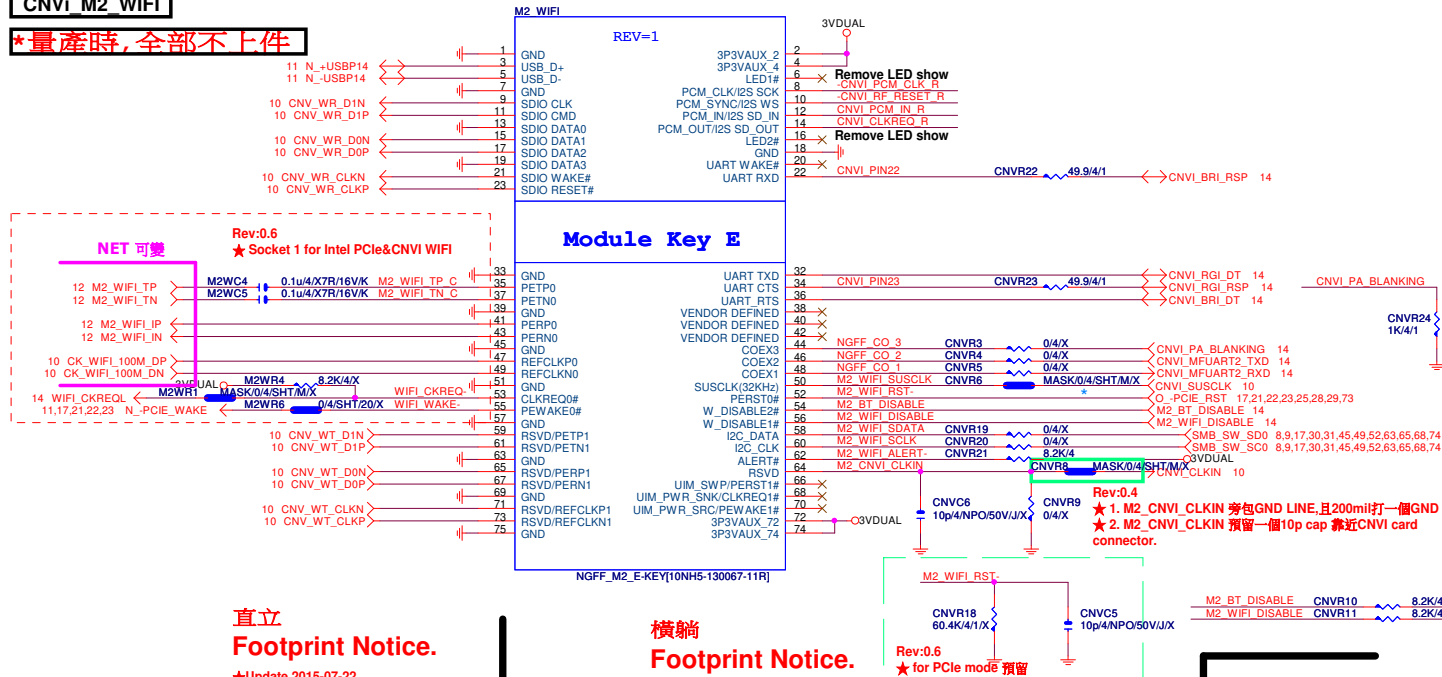
GROUP F



CNVi_M2_WIFI

*量產時,全部不上件

支援PCIE介面WIFI及USB介面BT



**直立
Footprint Notice.**

★Update 2015-07-22

★Footprint for 直立式 SMD:
WIFI-EKEY

★SMD P/N: 直立式
10NH5-130067-11R.

橫躺

Footprint Notice.

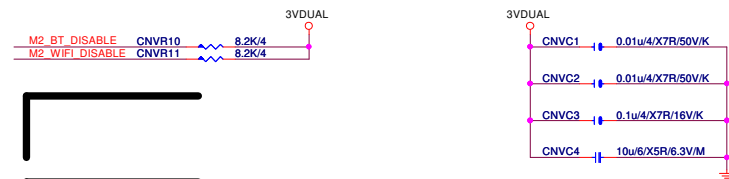
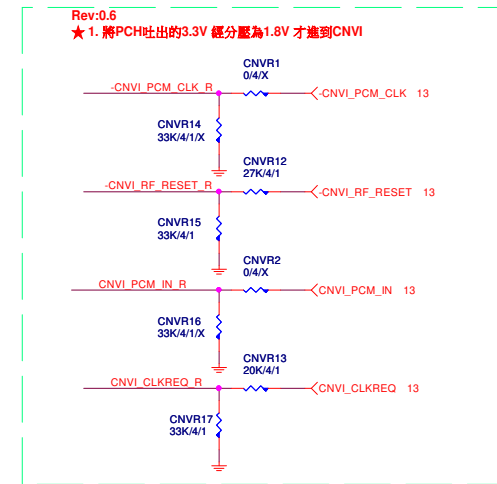
★Update 2015-07-22

★Footprint for 横躺式高:
NGFF-E-75P-3

★Footprint for 横躺式矮:
CNVI

★ 橫躺式高SMD
P/N:10NR5-130067-61R

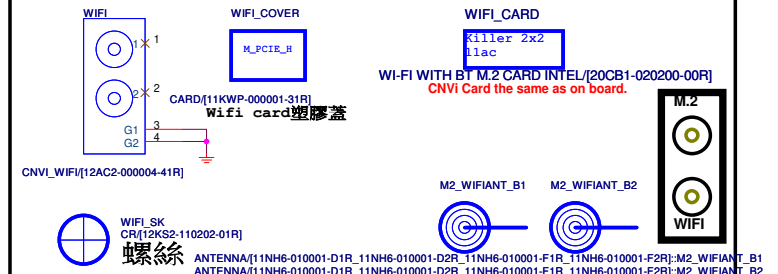
★ 橫躺式矮SMD
P/N:10NR5-130067-22R



FOR M.2 WIFI MODULE @ REAR PANEL

★Update 2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線

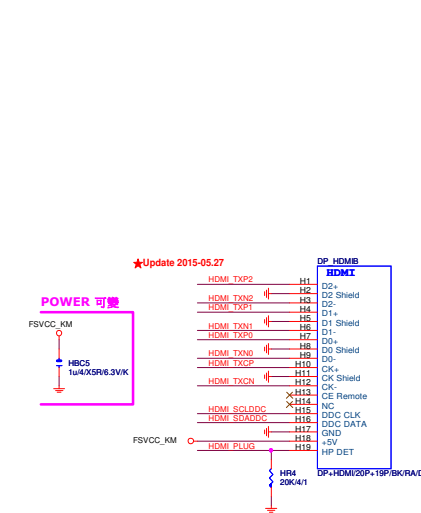


兩片式WIFI金屬殼改為單件式
Layout Library : wifi-ekey-module-1
Tiptop P/N : 12AC2-000004-31R

GIGABYTE™

Title	CNVi M2 WIFI
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Size Custom	Document Number B560 AORUS PRO AX	Rev 1.02
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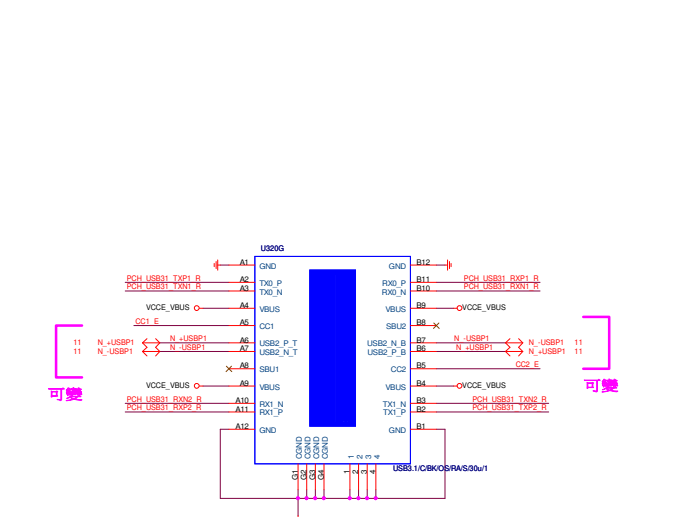
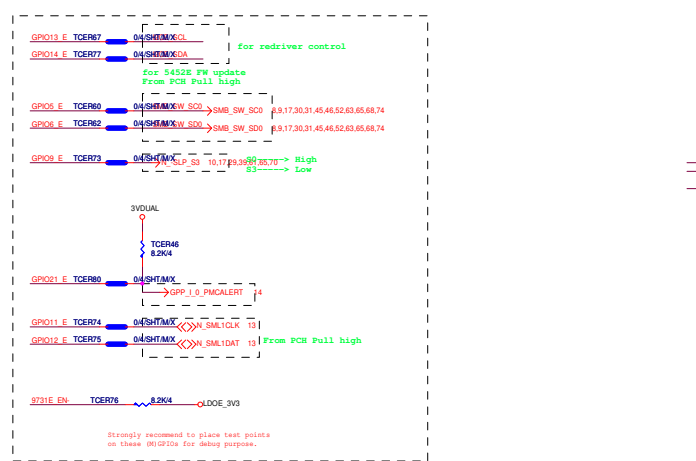
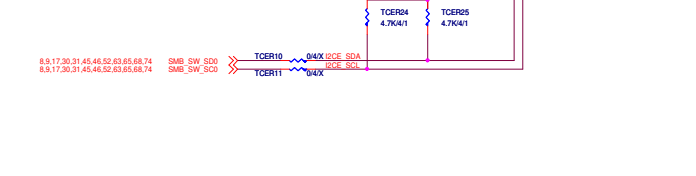
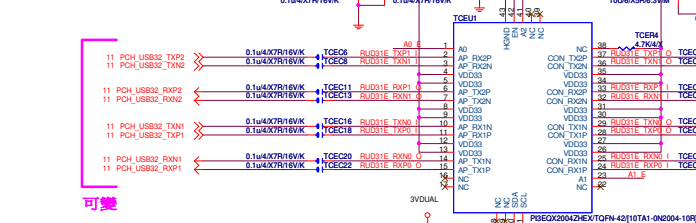


Gigabyte Technology			
Title			
HDMI _ NO LS/U32			
Size	Document Number	Rev	
Custom	Z590M GAMING X		1.0
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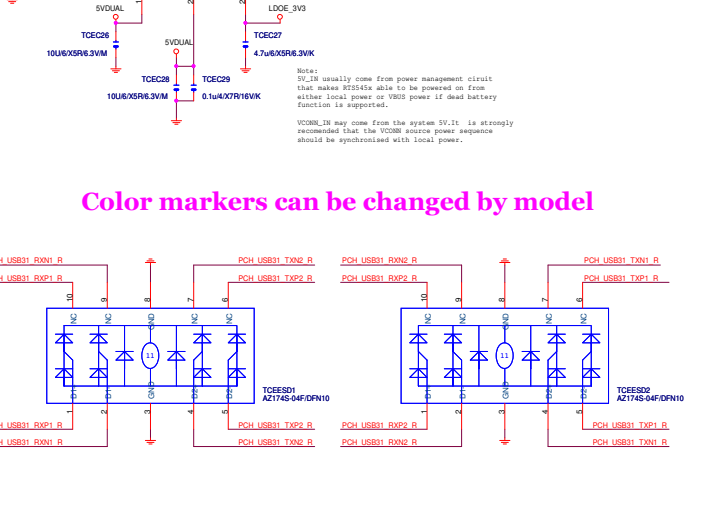
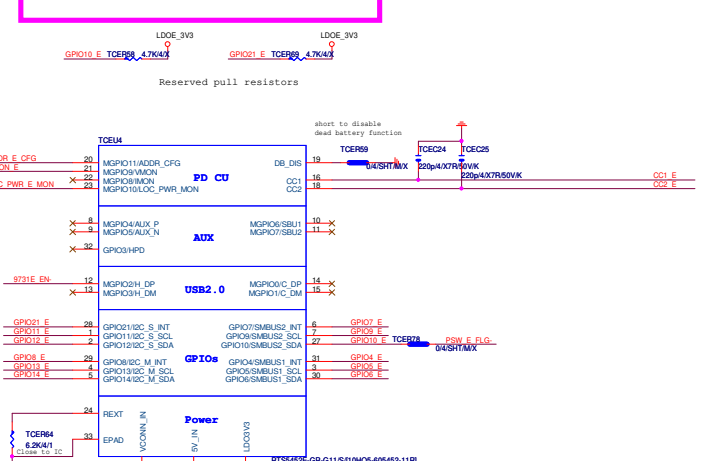
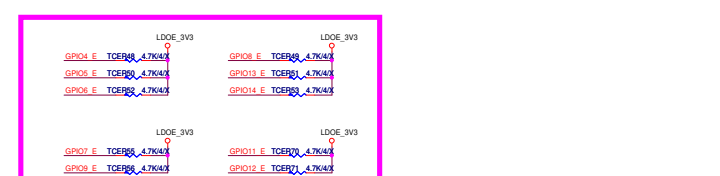
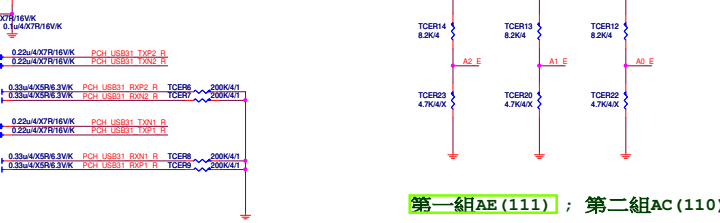
USB3.2 GEN2x2 PI3EQX2004 + RTS5452 Rev0.1

GROUP E

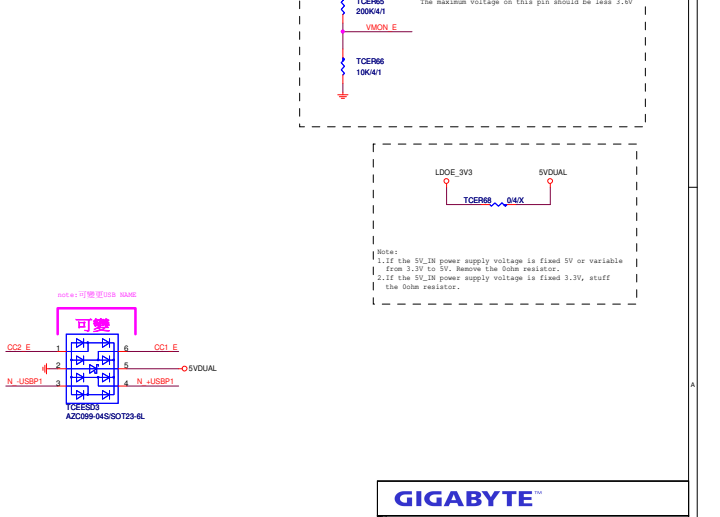
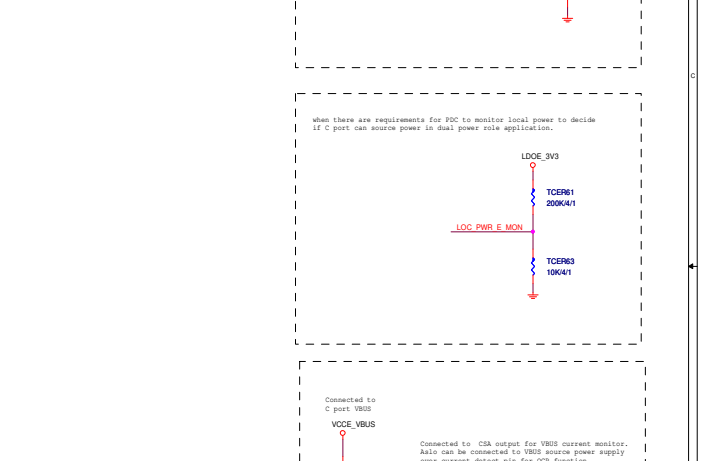
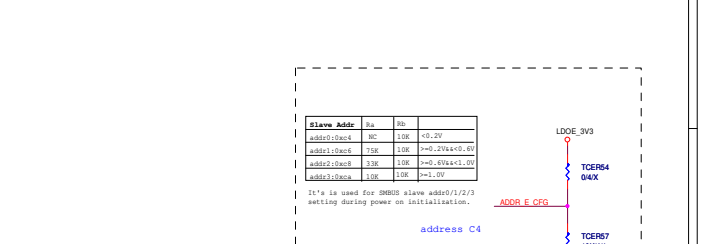
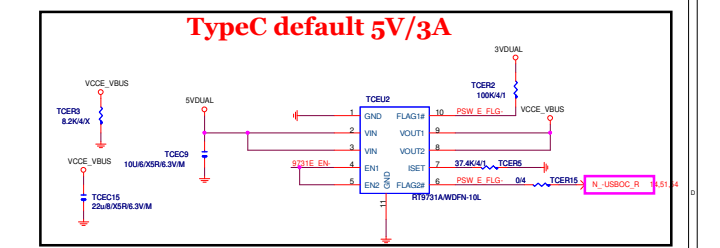
Rear TypeC



USB2.0 can be used the same source



Color markers can be changed by model

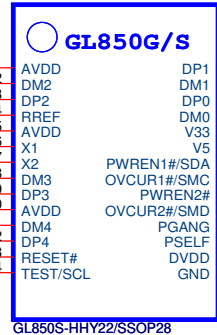


Color markers can be changed by model

Dual USB2 HUB used Rev 0.2

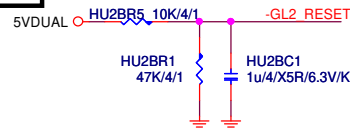
USB20 HUB_2

HUB2

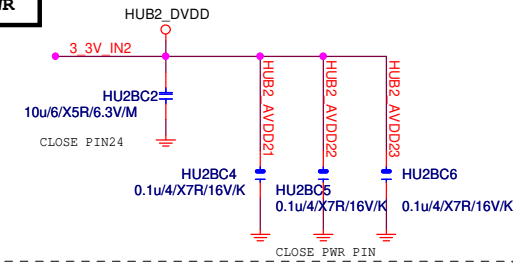


SSOP28-IT8209R

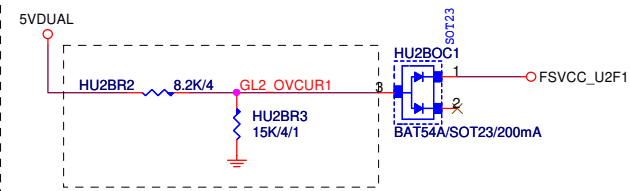
HUB RESET



HUB PWR

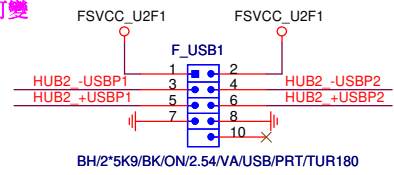


HUB OVER CURRENT SENSE



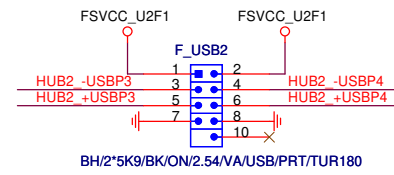
FRONT USB1

NET 可變



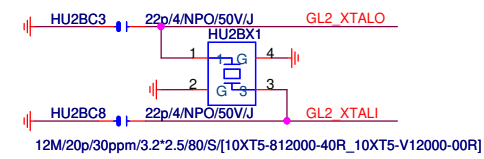
FRONT USB2

NET 可變



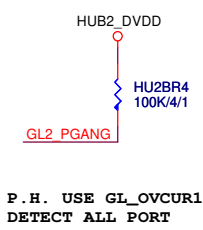
HUB CRYSTAL

ONLY SUPPORT 12MHZ

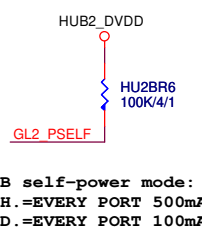


HUB MODE

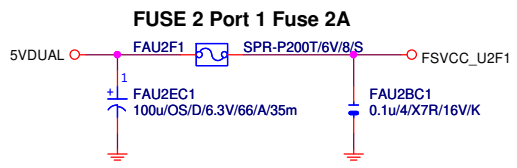
Ganged mode



PSELF



Close to connector
FUSE 2 Port 1 Fuse 2A



Close to connector
FUSE 2 Port 1 Fuse 2A

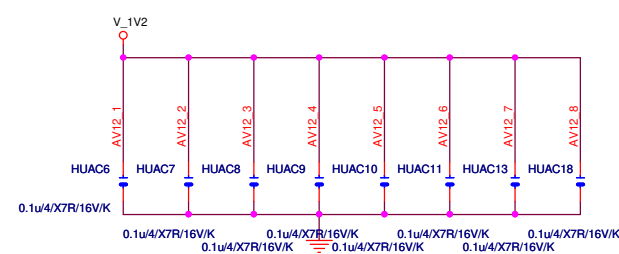
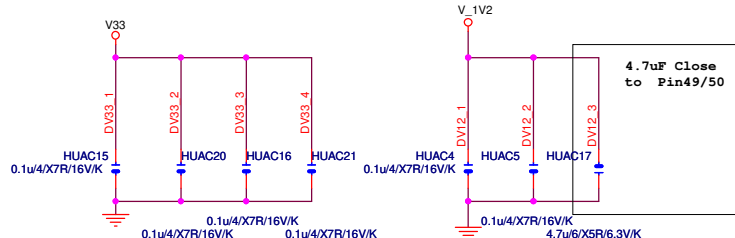
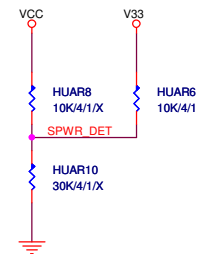
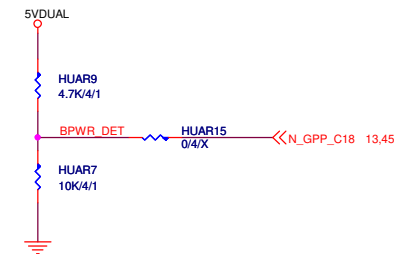
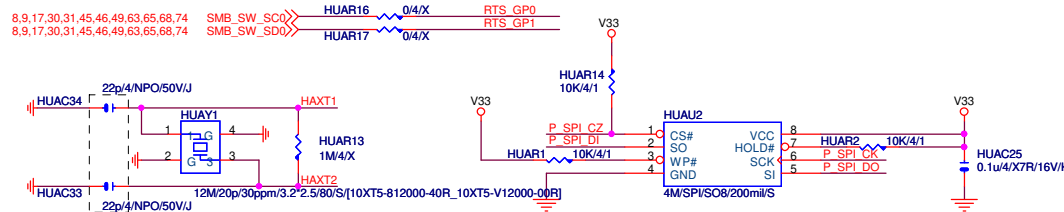
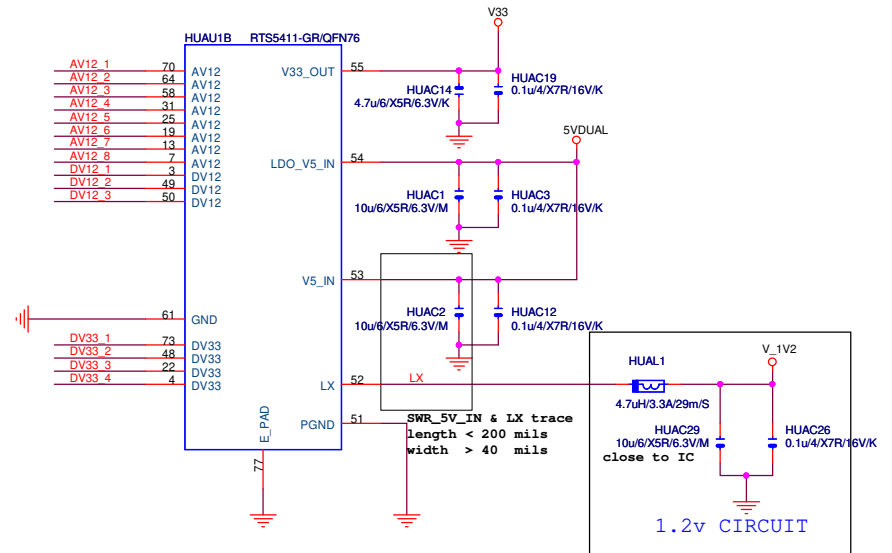
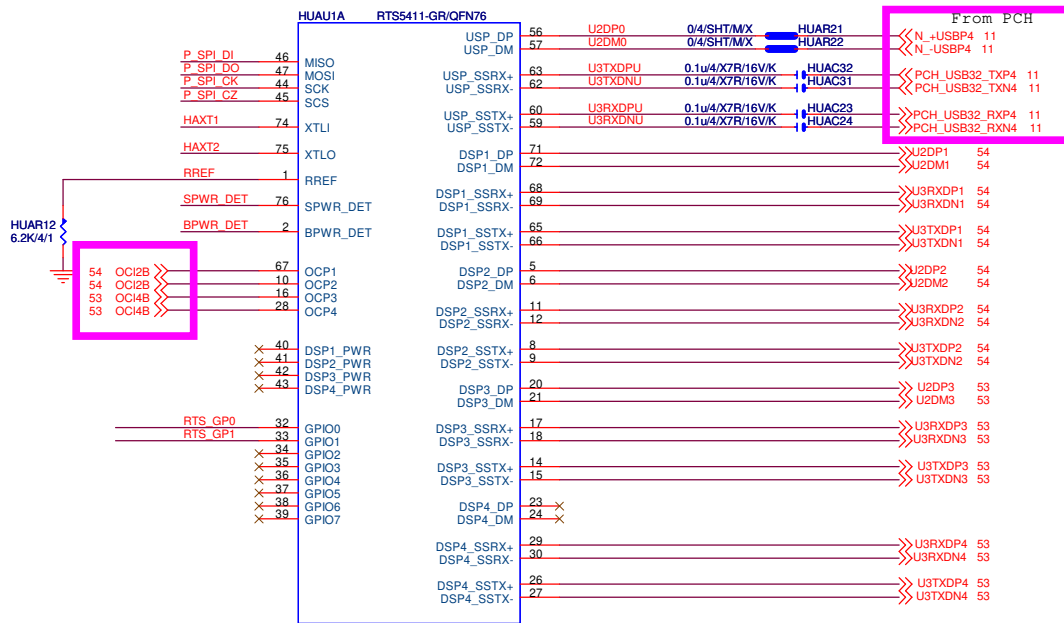
Gigabyte Technology

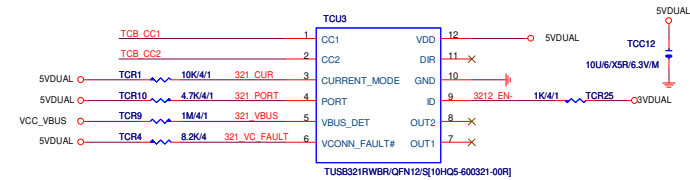
HUB GL850GS 1

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U32







CURRENT MODE

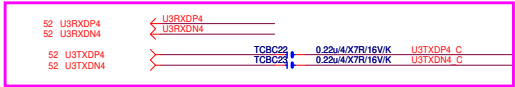
L - Default current / Pull down to GND or NC
M - Medium (1.5A) current / Pull up to VDD 500K
H - High (3.0A) current / Pull up to VDD 10K

PORT

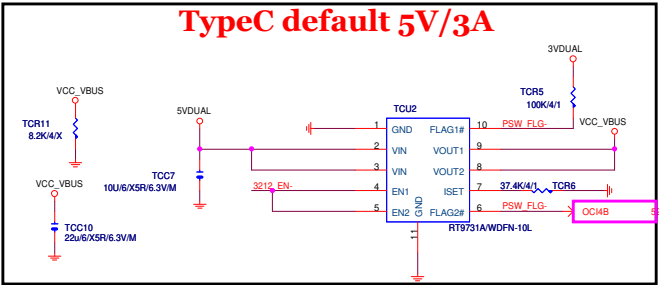
H - HOST
L - Device
NC - Dual Role

USB 3.x SuperSpeed

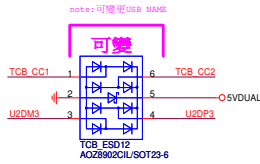
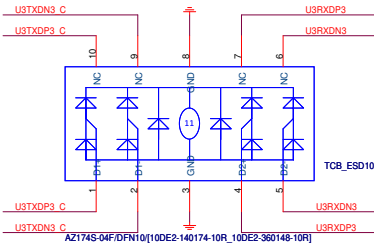
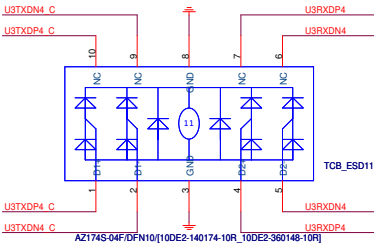
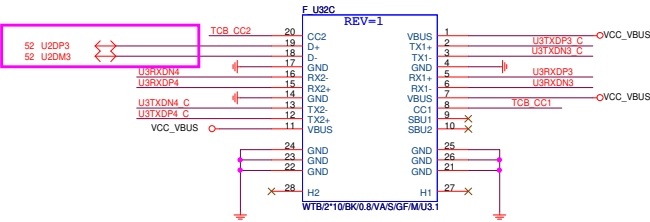
可變



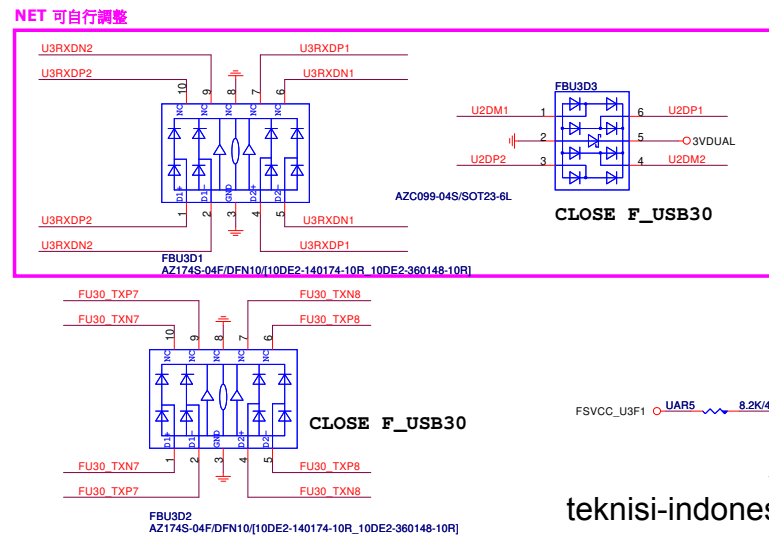
TypeC default 5V/3A



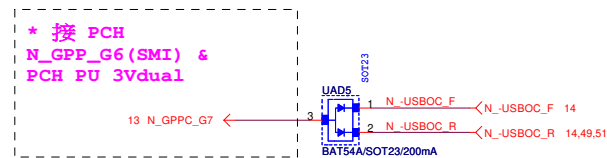
Color markers can be changed by model



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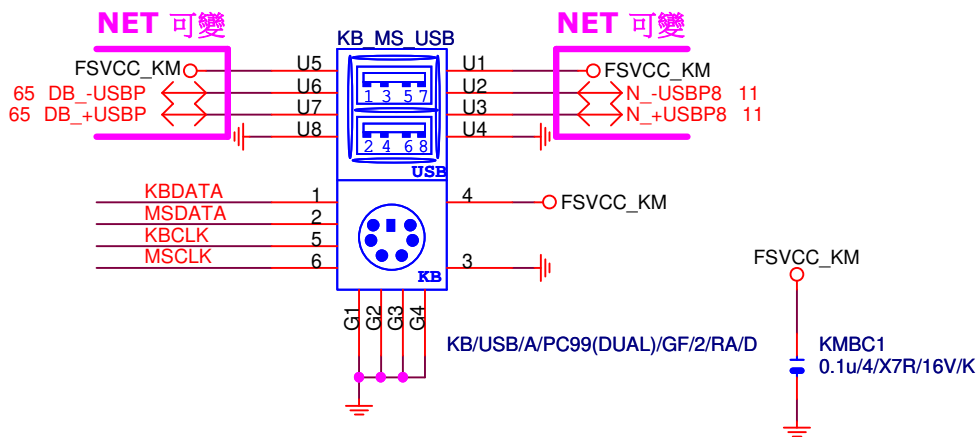


UAR5 8.2K/4 OCI2B 52

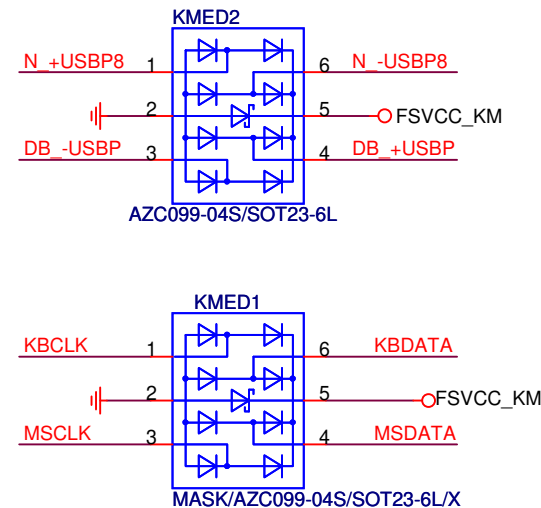


KB_MS_USB

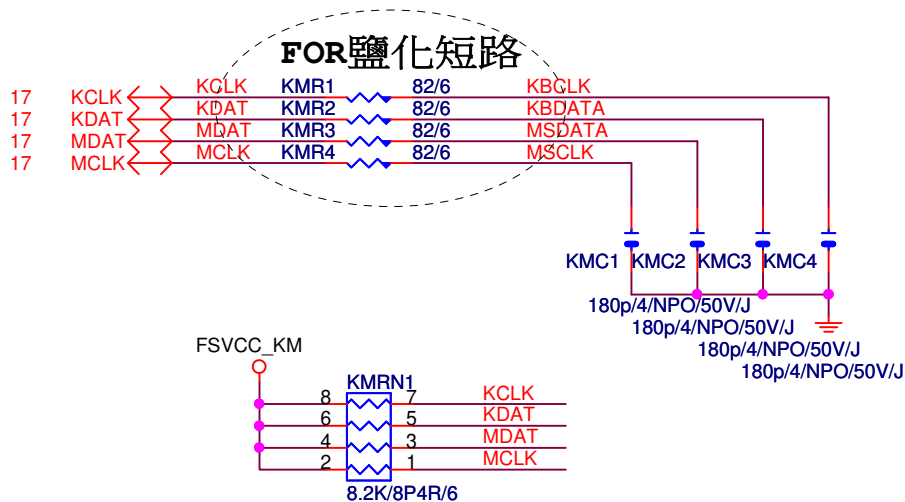
Rev: 0.7



ESD

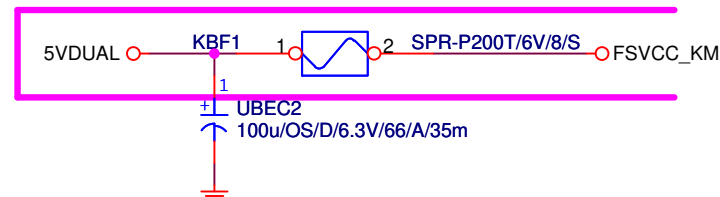


KB_MS_USB DAMPING/PU



KB_MS_USB PWR

NET 可變, 與其他USB SHARE



USB OC PROTECT

Gigabyte Technology

Title

KB_MS_USB30

Size

Document Number

Rev

B560 AORUS PRO AX

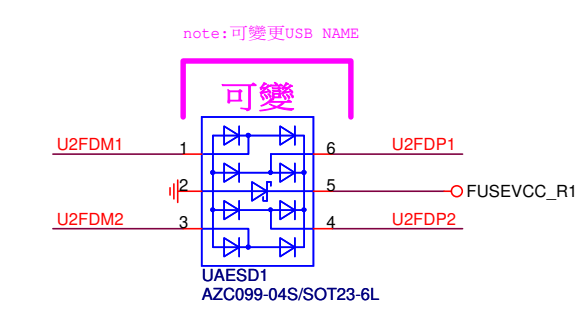
1.02

Date: Thursday, February 25, 2021

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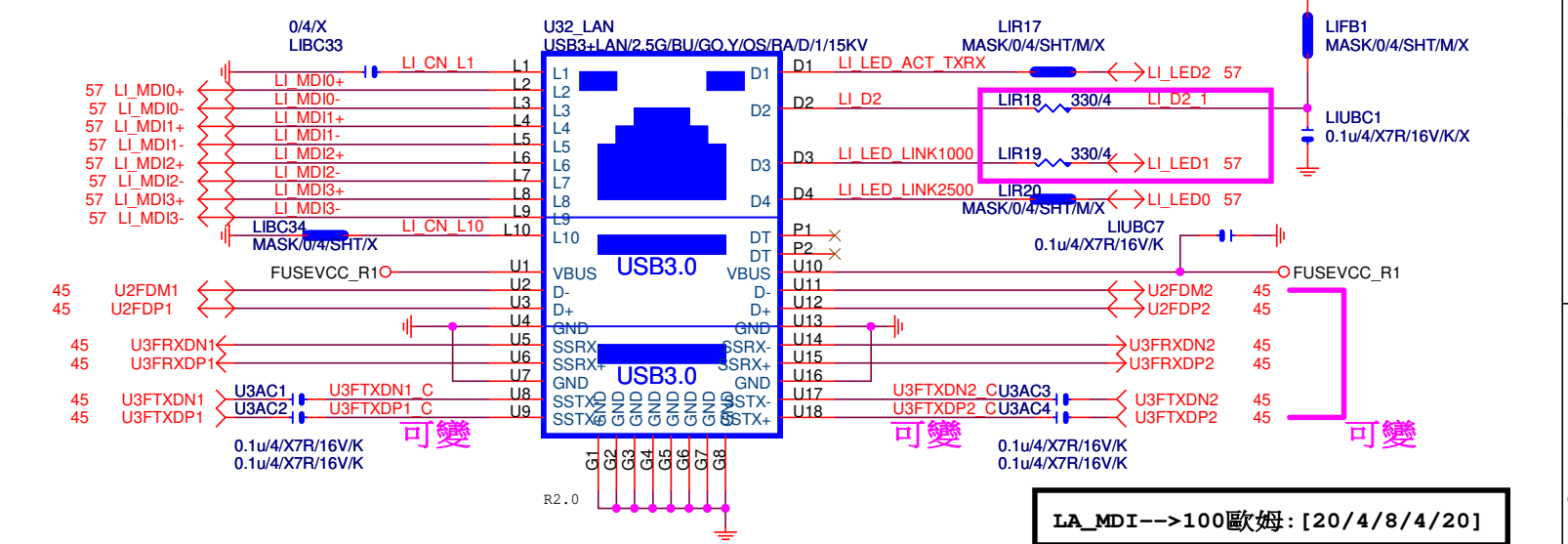
USB30_LAN CONNECTOR R1.02

RMA ESD PROTECT note:可變更USB NAME

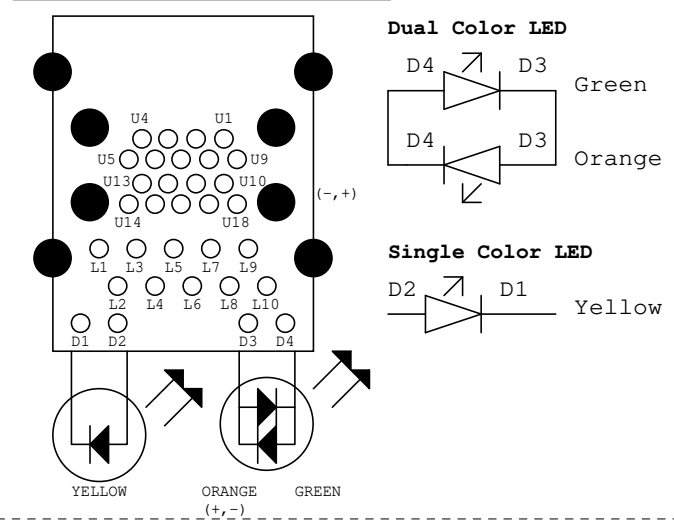


USB_LAN CONNECTOR note:可變更USB NAME

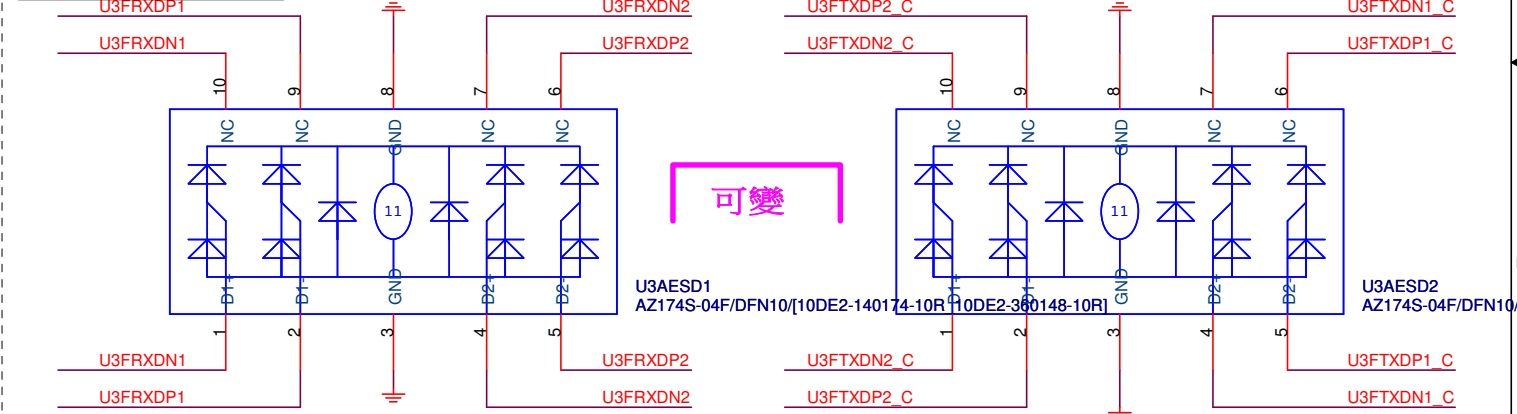
[I225]



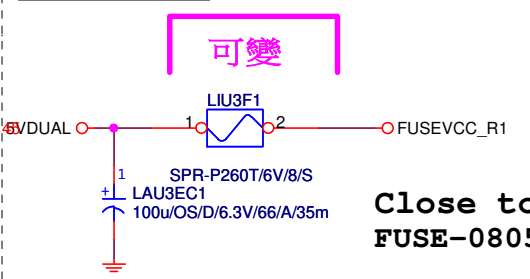
USB30_LAN LAYOUT示意图



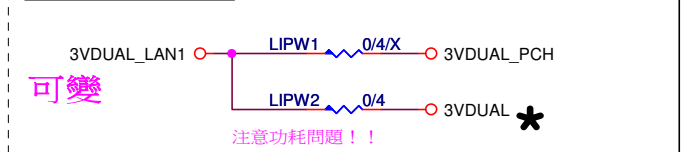
RMA ESD PROTECT note:可變更USB NAME



USB POWER note:可變更FUSE



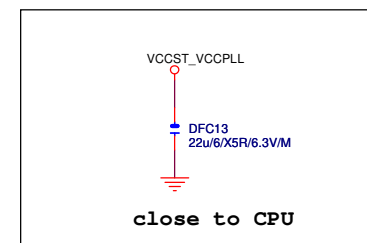
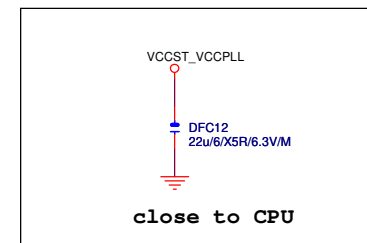
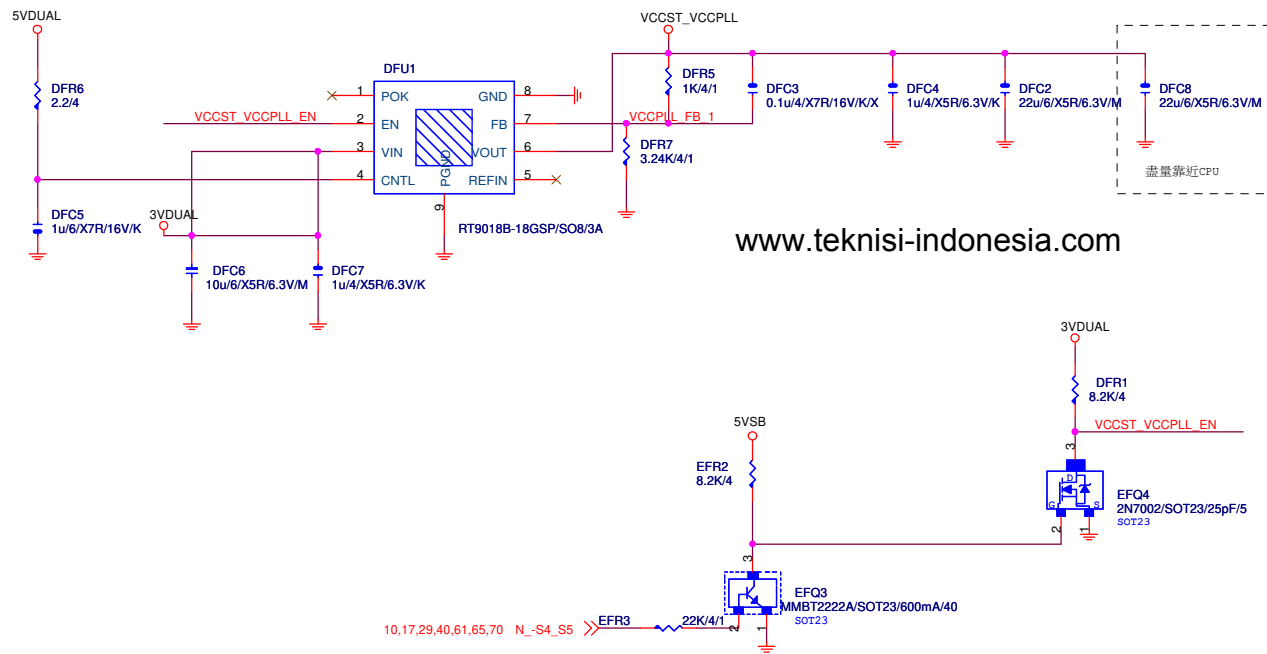
LAN POWER note: lan power連接及電流

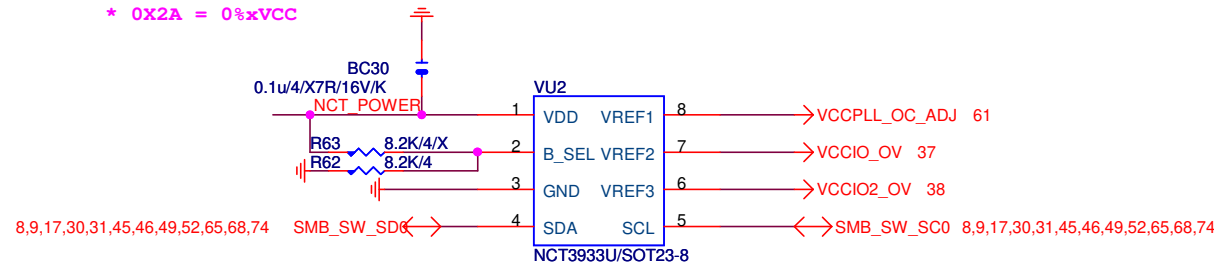
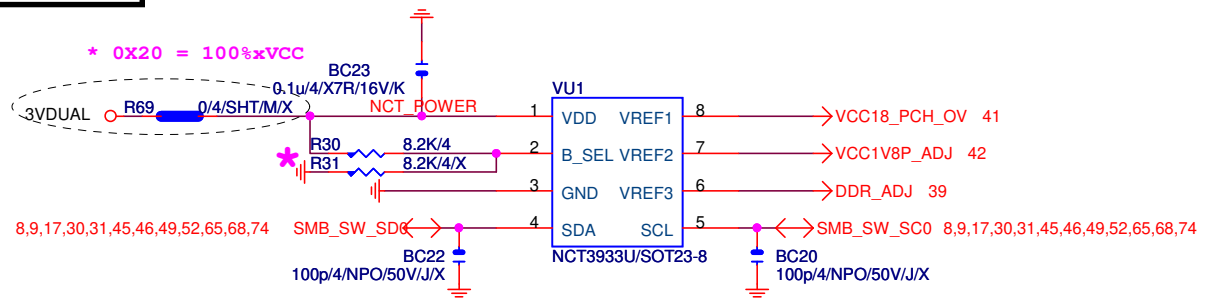




VCCST_VCCPLL

替換原先MOS開關線路





NCT3933	0X2A	0X20
VREF1	VCC18_PCH	VCCPLL_OC
VREF2	VCCIO	VCC1V8_PRIM
VREF3	VCCIO2	VDDQ

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TitleCPU CORE VR-2

Size Custom

Document Number

Rev

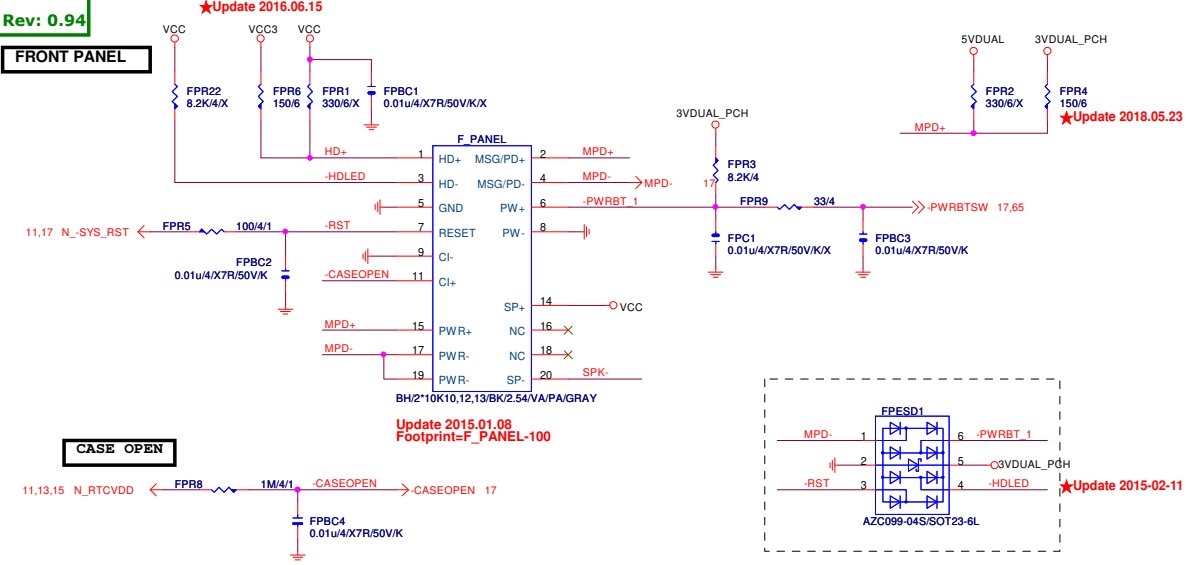
B560 AORUS PRO AX

1.02

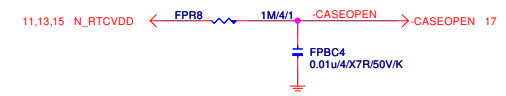
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FRONT PANEL

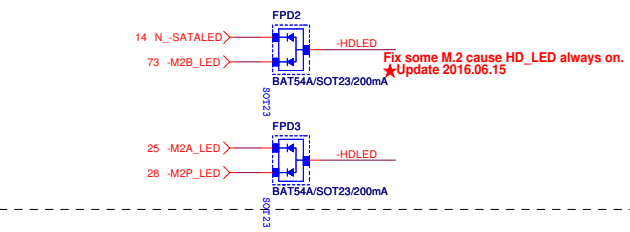


CASE OPEN

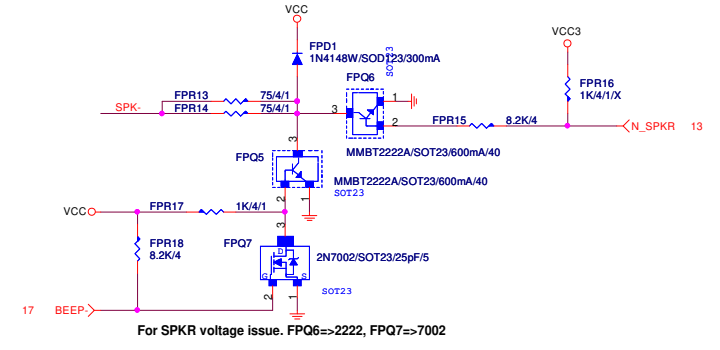


FRONT PANEL SHORT

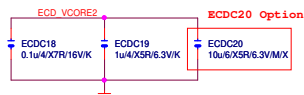
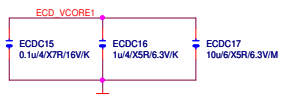
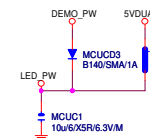
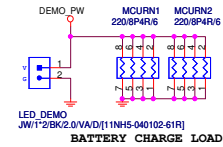
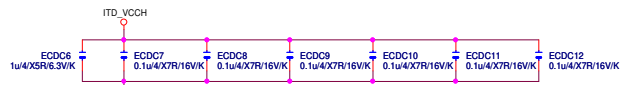
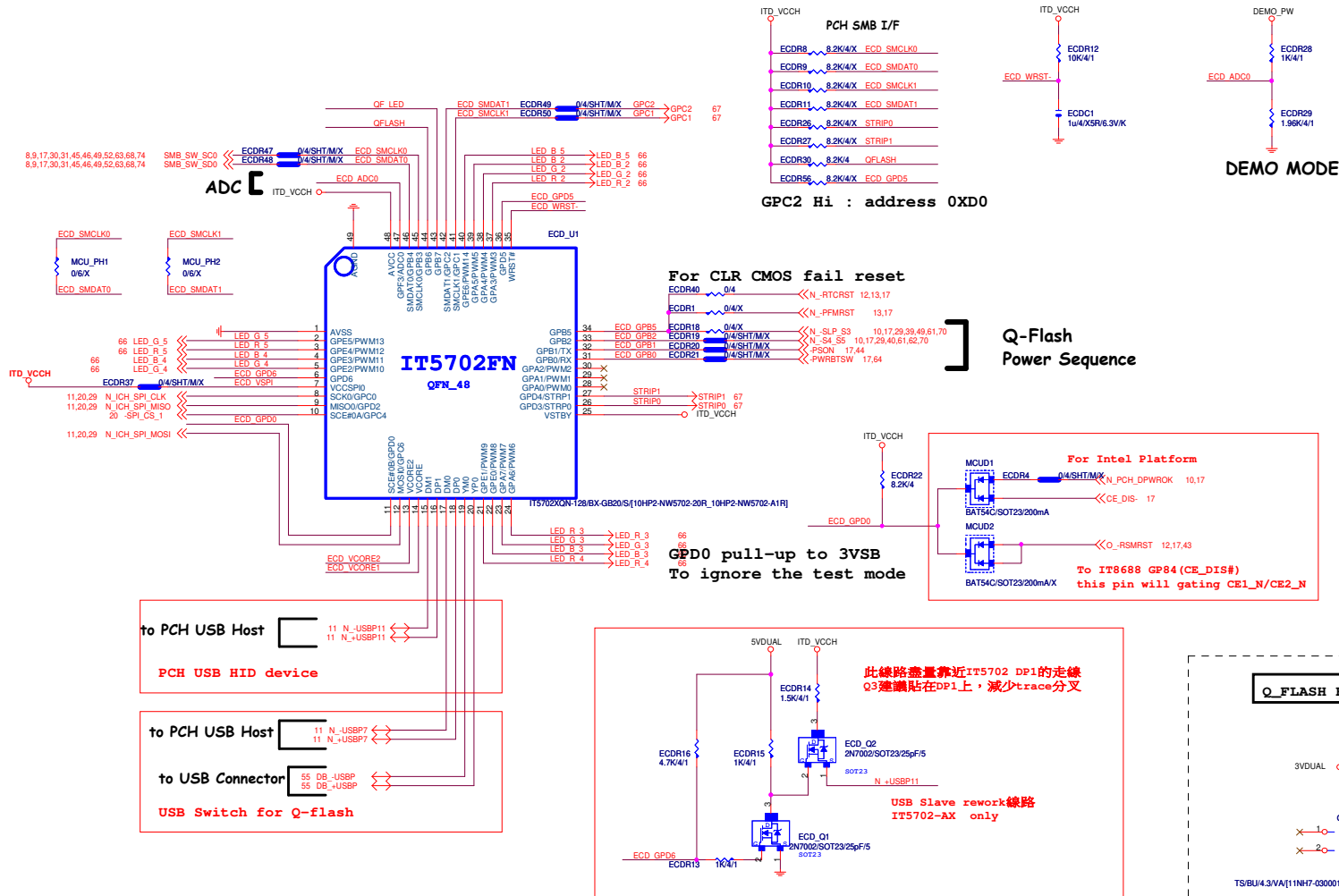
SATA/M.2 LED



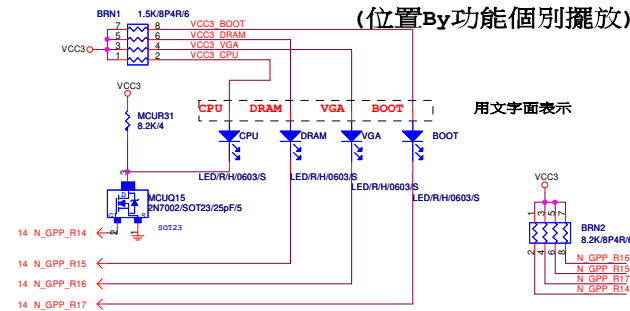
SPKR W/O EC



ECD_U1 請放在PCH到BIOS路徑上. 避免線過長



DEBUG PORT LED *4
(位置By功能個別擺放)



N_GPP_R14	CPU DEBUG
N_GPP_R15	DDR DEBUG
N_GPP_R16	VGA DEBUG
N_GPP_R17	BOOT DEVICE DEBUG

第三區 LED

第三區 LED CONTROL

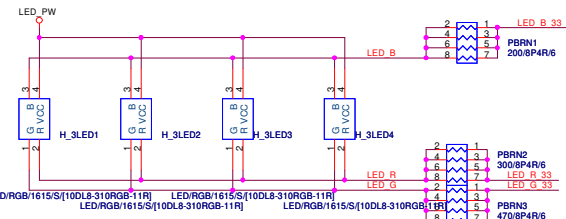
第五區 LED

第二區 LED CONTROL

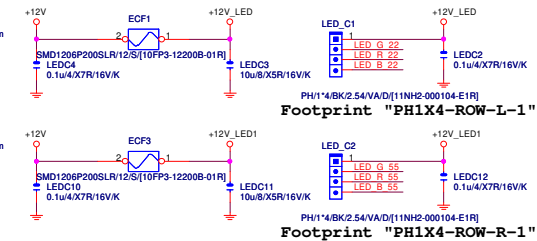
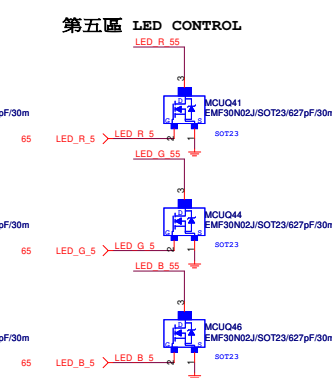
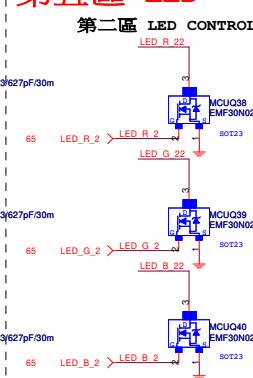
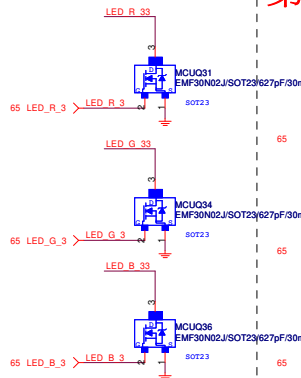
第五區 LED CONTROL

燈條 LED (LED_C1放在PCB左邊板邊位置)
燈條 LED (LED_C2放在PCB右邊板邊位置)

FOR PCH 正發光 LED*6 (位置在正板, 依據PCH_HS設計擺放)



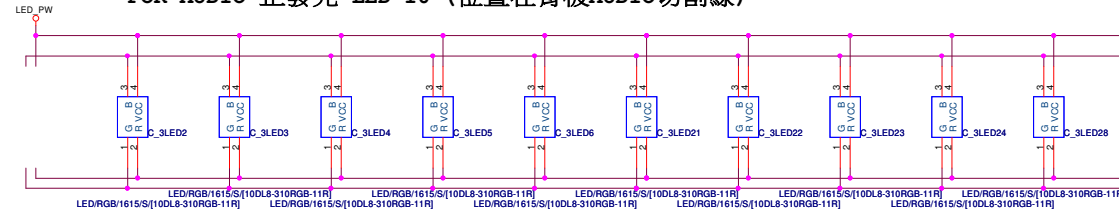
FOOTPRINT: LED-4P-RGB



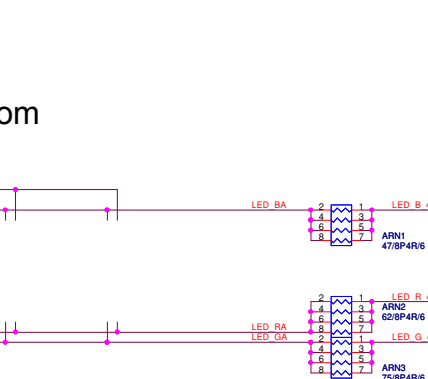
第四區 LED

第四區 LED CONTROL

FOR AUDIO 正發光 LED*10 (位置在背板AUDIO切割線)



FOOTPRINT: LED-4P-RGB

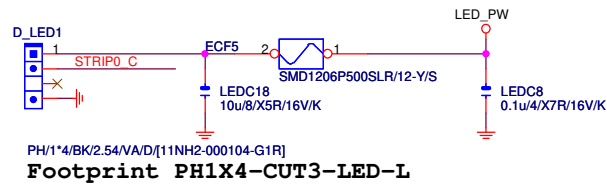


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File PCH/AUDIO/DEBUG/C_LED1/2		
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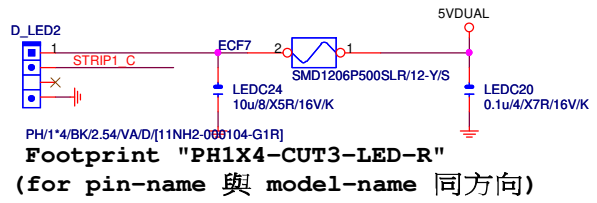
第六區 LED (靠近左上板邊位置)

Digital LED Strip1

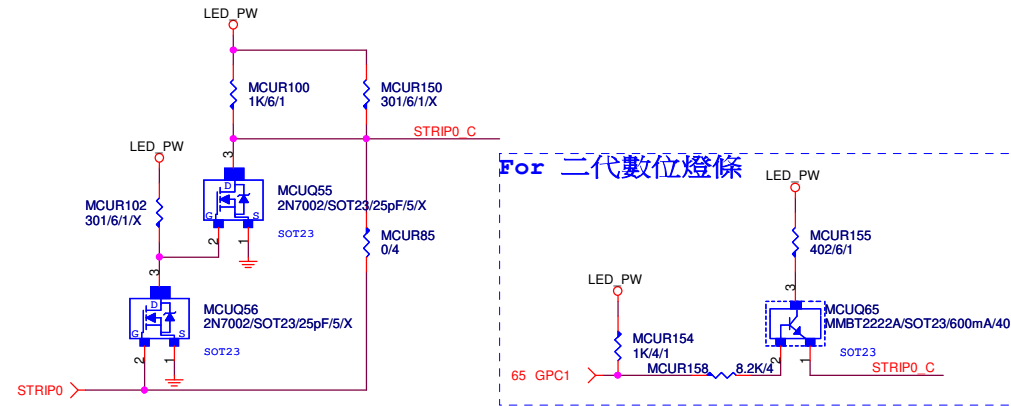


第七區 (靠近右下CPU板邊位置)

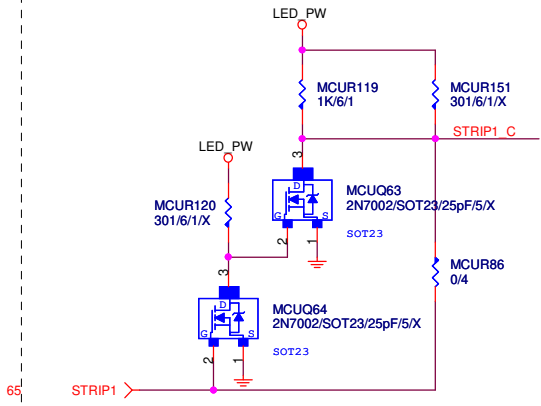
Digital LED Strip2



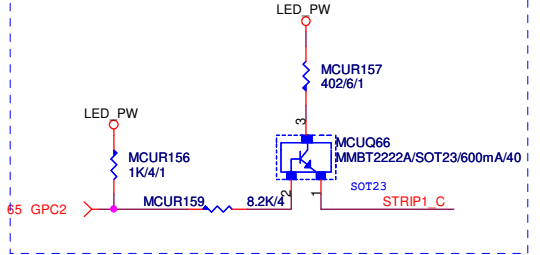
燈條 Level shift

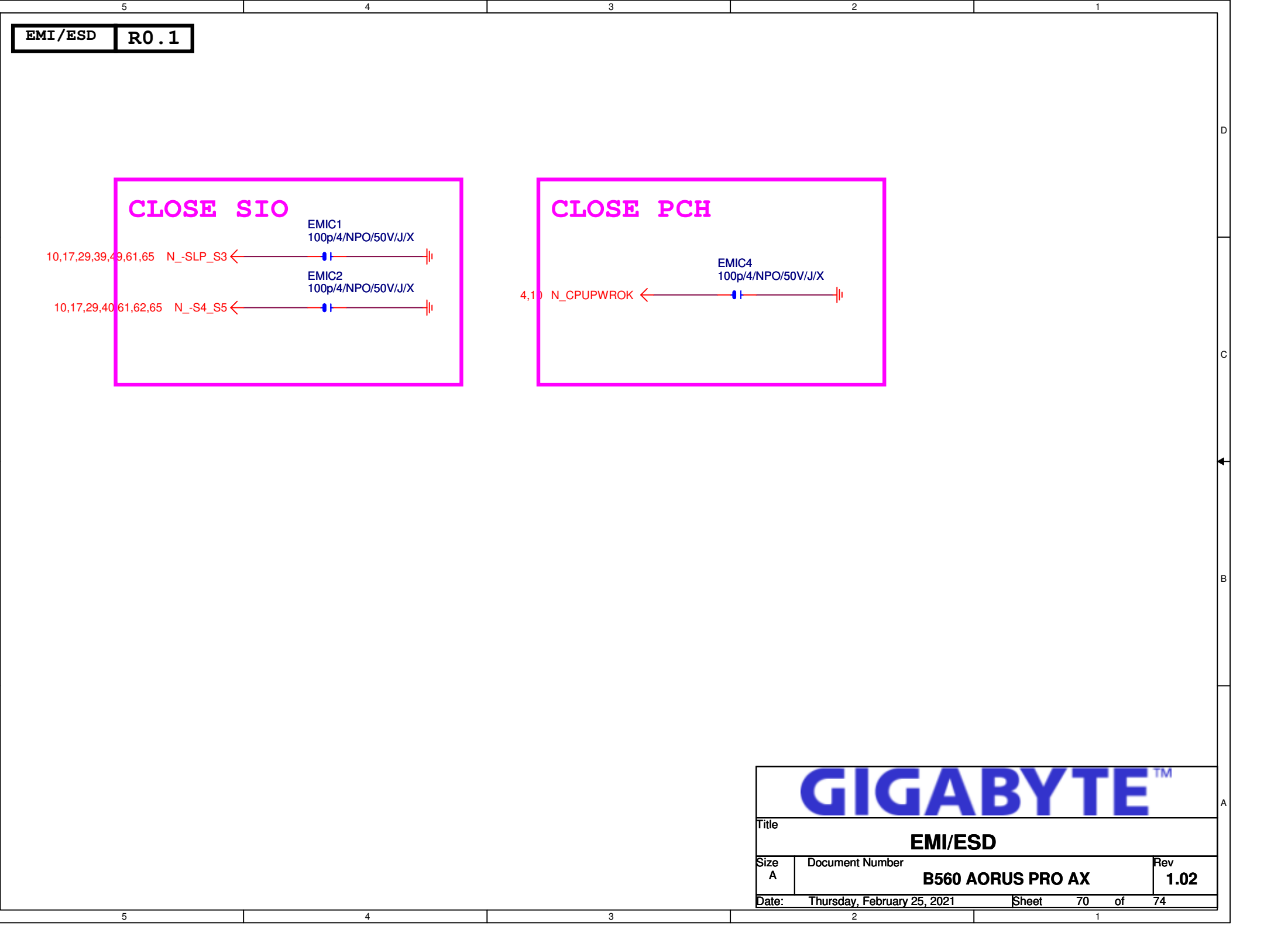


燈條 Level shift

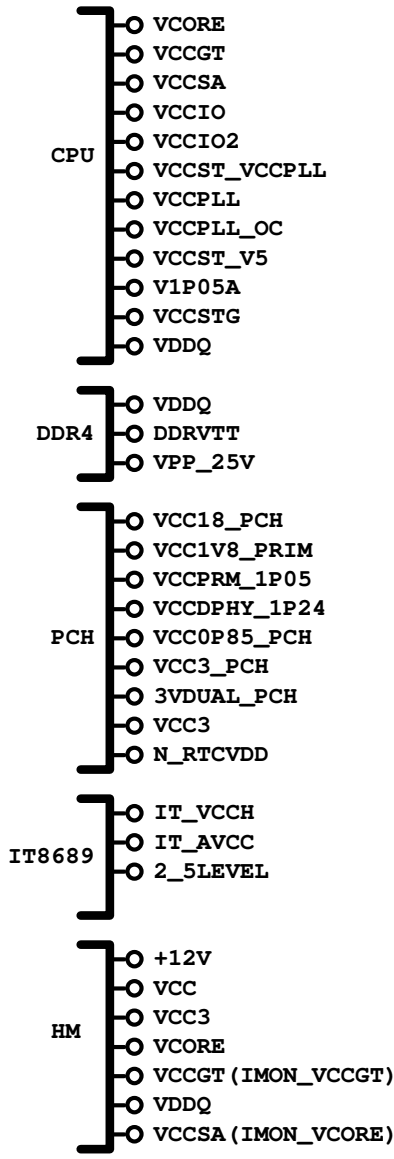


For 二代數位燈條

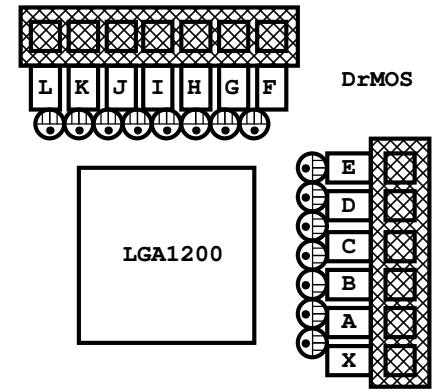
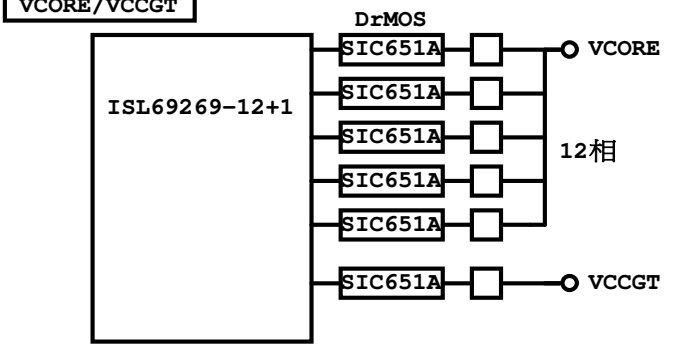




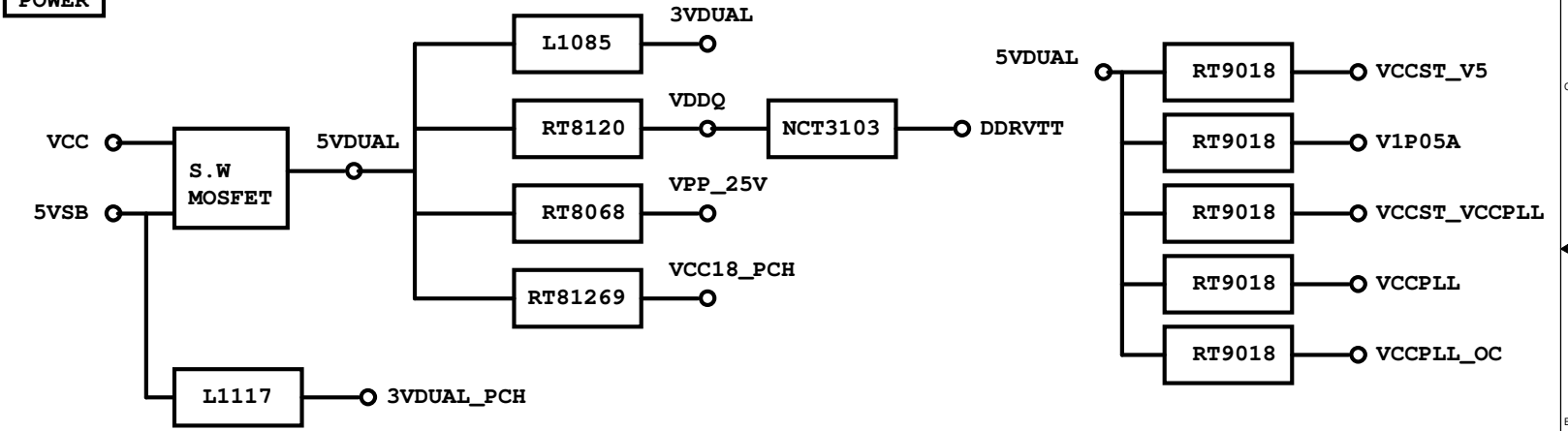
POWER BLOCK MAP



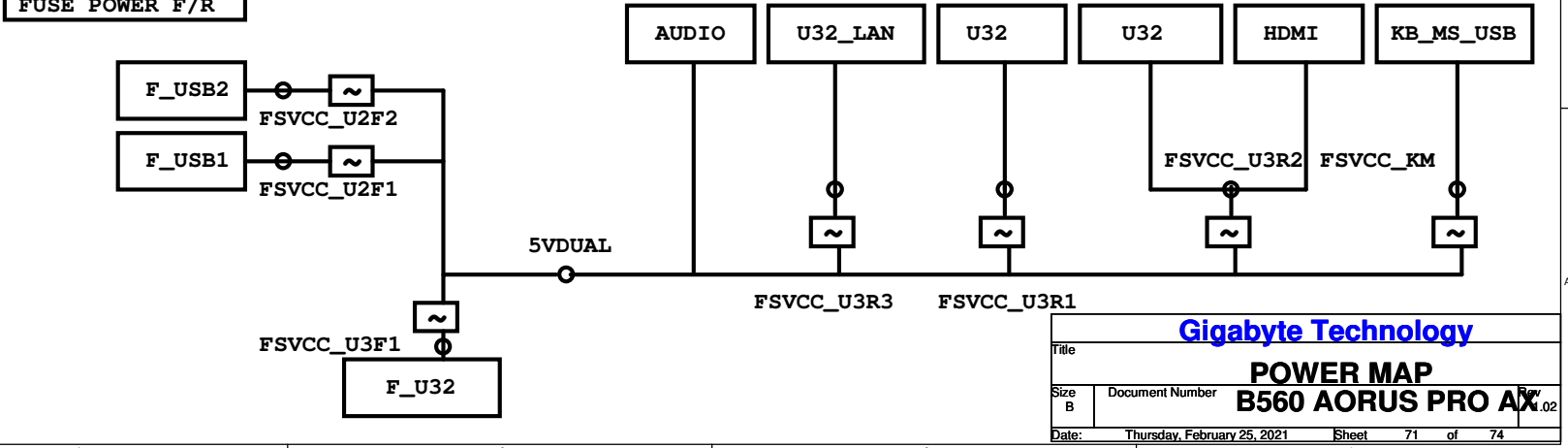
VCORE/VCCGT

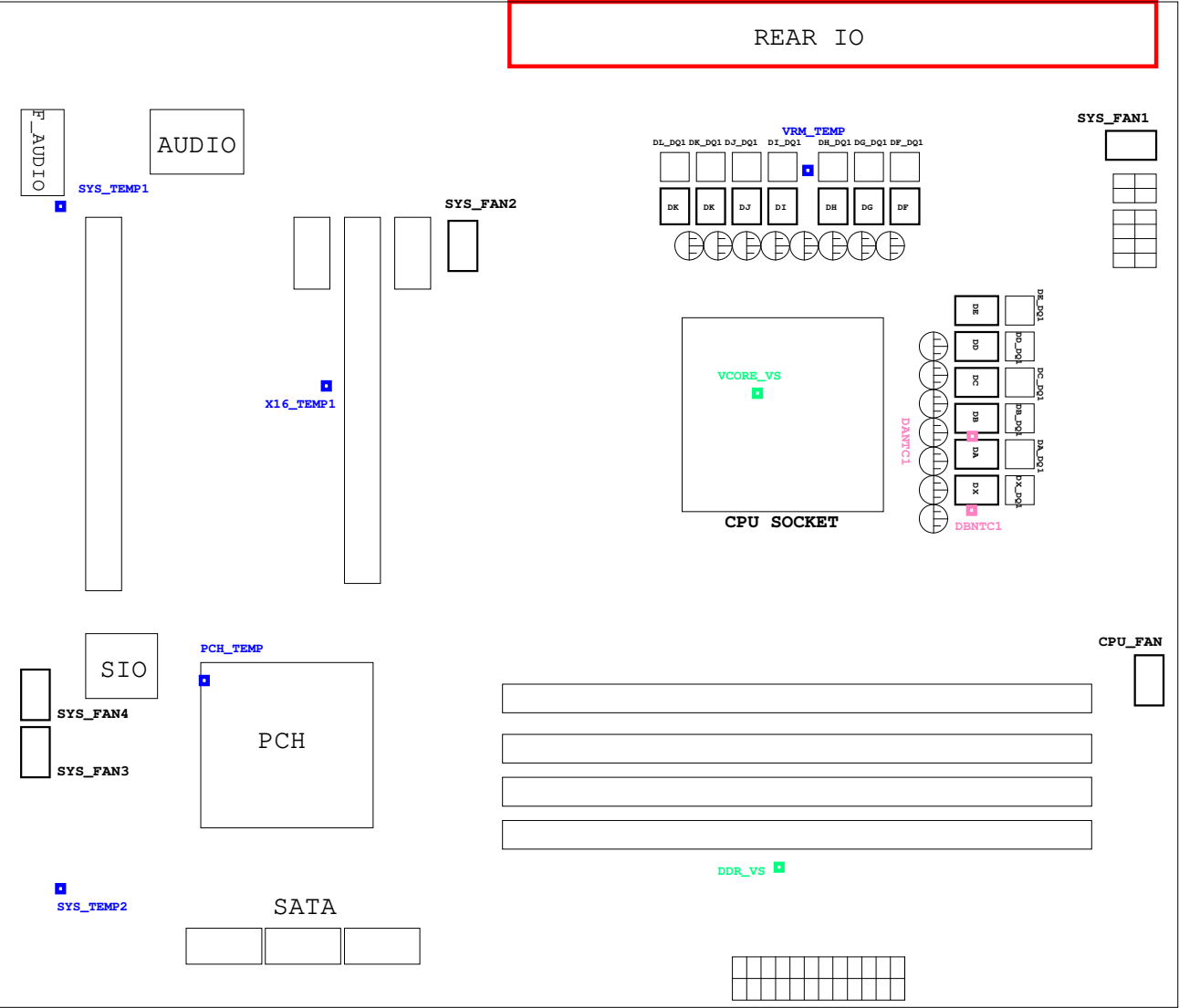


POWER



FUSE POWER F/R





熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL2	Differential
DANTC2	DA_DQ3	Differential
DANTC3	DM_DQ2	Differential
DANTC4	DM_DL1	Differential
VRM_TEMP	DC_DQ1	N/A
X16_TEMP1	PCIEX16	N/A
PCH_TEMP	PCH	N/A
SYS_TEMP1	F_AUDIO	N/A
SYS_TEMP2	F_PANEL	N/A

■ SIO RS
■ PWM RS
■ SIO VIN

■ FAN

Rev 0.6

M.2 Lane3 from PCH port24

M.2 Lane2 from PCH port23

M.2 Lane1 from PCH port22

M.2 Lane1 from PCH port21

支援SATA and M.2 function

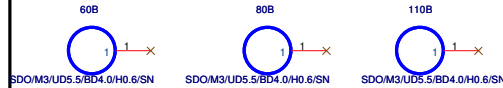
需與M2_-CLKREQ對應

架高 金屬加強

Footprint : m2_110_h2mm8w

SMD螺母

10KS2-040131-01R



DIP螺柱

有上M2 HEATSINK時螺柱/螺母一體式



架高

有上M2 HEATSINK時特制螺絲



DIP螺絲

M2_SB_HS

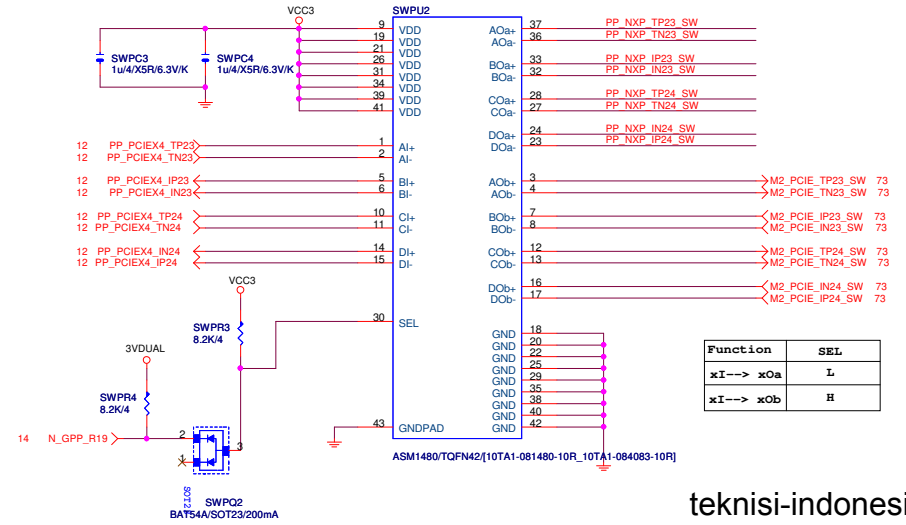
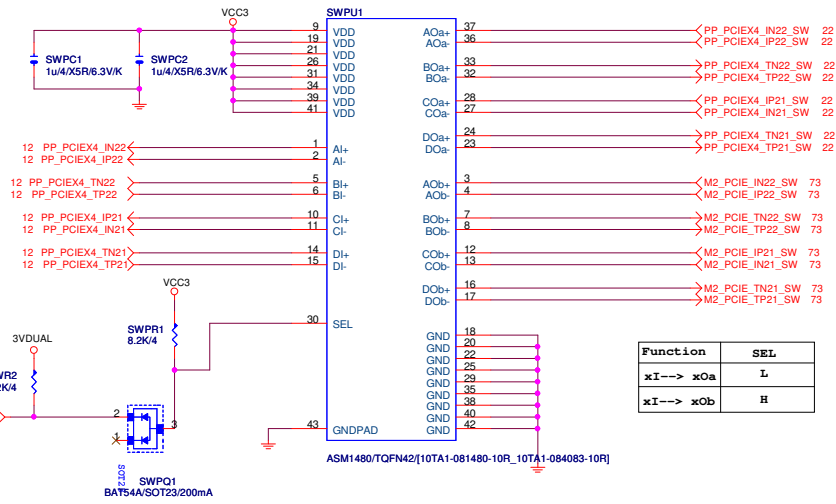
M2 HEATSINK

M2_SB_HS/[12SP1-S11705-02R_12SP1-S11705-04R_12SP1-S11705-05R]:M2_SB_HS

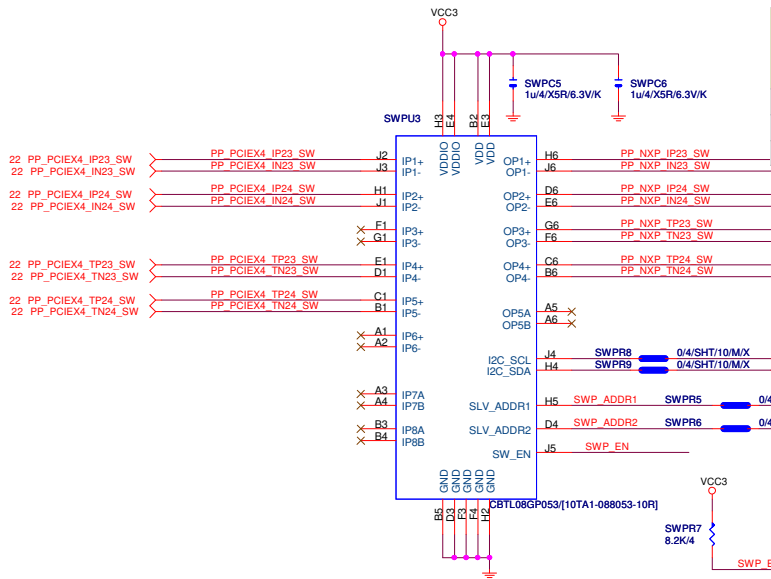
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M2P / PCIe4	GPI			GPO		M.E. Config				CBT108GP053	
	N_GPP_F19	N_GPP_F20	N_GPP_D13	N_GPP_F21	N_GPP_F22	P24	P23	P22	P21	0x60/0x61	
M.2x4	0	1	1	1	1	PCIEx4				Don't Care	
PCIEx4	1	1	0	0	0	PCIEx4 (Reverse)				IP1=OP1, IP2=OP2, IP4=OP3, IP5=OP4	
M.2x2+PCIEx2	0	1	0	1	0	PCIEx2		PCIEx2		IP2=OP1, IP1=OP2, IP5=OP3, IP4=OP4	

Table 5. Device slave address

SLV_ADDR2	SLV_ADDR1	PC-bus device address
LOW	LOW	0x60/0x61
LOW	HIGH	0x64/0x65
HIGH	LOW	0x68/0x69
HIGH	HIGH	0x6C/0x6D

Gigabyte Technology SWITCH			
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